

DETAILED DESCRIPTION

General

The Si4320 FSK receiver is the counterpart of the Si4220 FSK transmitter. It covers the unlicensed frequency bands at 315, 433, 868, and 915 MHz. The device facilitates compliance with FCC and ETSI requirements.

The receiver employs the Zero-IF approach with I/Q demodulation, allowing the use of a minimal number of external components in a typical application. The Si4320 consists of a fully integrated multi-band PLL synthesizer, an LNA with switchable gain, I/Q down converter mixers, baseband filters and amplifiers, and an I/Q demodulator followed by a data filter.

PLL

The programmable PLL synthesizer determines the operating frequency, while preserving accuracy based on the on-chip crystal-controlled reference oscillator. The PLL's high resolution allows for the use of multiple channels in any of the bands.

The RF VCO in the PLL performs automatic calibration, which requires only a few microseconds. Calibration always occurs when the synthesizer begins. If temperature or supply voltage changes significantly or operational band has changed, VCO recalibration is recommended. Recalibration can be initiated at any time by switching the synthesizer off and back on again.

LNA

The LNA has 250 Ohm input impedance, which works well with the recommended antennas. (See Application Notes available from www.silabs.com/integration.)

If the RF input of the chip is connected to 50 Ohm devices, an external matching circuit is required to provide the correct matching and to minimize the noise figure of the receiver.

The LNA gain (and linearity) can be selected (0, -6, -14, -20 dB relative to the highest gain) according to RF signal strength. This is useful in an environment with strong interferers.

Baseband Filters

The receiver bandwidth is selectable by programming the bandwidth (BW) of the baseband filters. This allows setting up the receiver according to the characteristics of the signal to be received.

An appropriate bandwidth can be selected to accommodate various FSK deviation, data rate, and crystal tolerance requirements. The filter structure is a 7-th order Butterworth low-pass with 40 dB suppression at 2*BW frequency. Offset cancellation is accomplished by using a high-pass filter with a cut-off frequency below 7 kHz. See Measurement Results section for measured receiver selectivity curves.

Data Filtering and Clock Recovery

The output data filtering can be completed by an external capacitor or by using digital filtering according to the final application.

Analog operation: The filter is an RC type low-pass filter and a Schmitt-trigger (St). The resistor (10k) and the St is integrated on the chip. An (external) capacitor can be chosen according to the actual bit-rate. In this mode the receiver can handle up to 256 kbps data rate.

Digital operation: The data filter is a digital realization of an analog RC filter followed by a comparator with hysteresis. In this mode there is a clock recovery circuit (CR), which can provide synchronized clock to the data. With this clock the received data can fill the RX Data FIFO. The CR has three operation modes: fast, slow, and automatic. In slow mode, its noise immunity is very high, but it has slower settling time and requires more accurate data timing than in fast mode. In automatic mode the CR automatically changes between fast and slow modes. The CR starts in fast mode, then automatically switches to slow mode after locking.

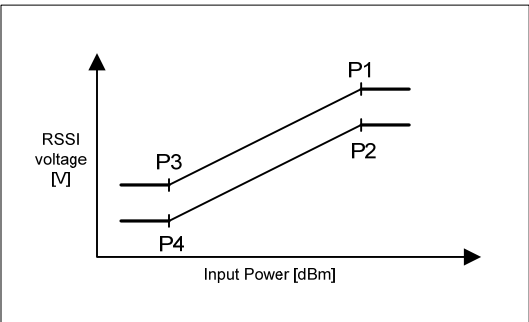
(Only the data filter and the clock recovery use the bit-rate clock. Therefore, in analog mode, there is no need for setting the correct bit-rate.)

Data Validity Blocks

RSSI

A digital RSSI output is provided to monitor the input signal level. It goes high if the received signal strength exceeds a given preprogrammed level. An analog RSSI signal is also available. The RSSI settling time depends on the filter capacitor used.

Voltage on ARSSI pin vs. Input RF power



P1	-65 dBm	1300 mV
P2	-65 dBm	1000 mV
P3	-100 dBm	600 mV
P4	-100 dBm	300 mV

DQD

The Data Quality Detector monitors the I/Q output of the baseband amplifier chain by counting the consecutive correct 0->1, 1->0 transitions. The DQD output indicates the quality of the signal to be demodulated. Using this method it is possible to "forecast" the probability of BER degradation. The programmable DQD parameter defines the threshold for signaling the good/bad data quality by the digital one-bit DQD output. In cases when the deviation is close to the bitrate, there should be four transitions during a single one bit period in the I/Q signals. As the bitrate decreases in comparison to the deviation, more and more transitions will happen during a bitperiod.

AFC

By using an integrated Automatic Frequency Control (AFC) feature, the receiver can synchronize its local oscillator to the received signal, allowing the use of:

- inexpensive, low accuracy crystals
- narrower receiver bandwidth (i.e. increased sensitivity)
- higher data rate

Crystal Oscillator

The chip has a single-pin crystal oscillator circuit, which provides a 10 MHz reference signal for the PLL. To reduce external parts and simplify design, the crystal load capacitor is internal and programmable. Guidelines for selecting the appropriate crystal can be found later in this datasheet. The receiver can supply the clock signal for the microcontroller, so accurate timing is possible without the need for a second crystal.

When the microcontroller turns the crystal oscillator off by clearing the appropriate bit using the Configuration Setting Command, the chip provides a fixed number (128) of further clock pulses ("clock tail") for the microcontroller to let it go to idle or sleep mode.

Low Battery Voltage Detector

The low battery detector circuit monitors the supply voltage and generates an interrupt if it falls below a programmable threshold level. The detector circuit has 50 mV hysteresis.

Wake-Up Timer

The wake-up timer has very low current consumption (1.5 μ A typical) and can be programmed from 1 ms to several days with an accuracy of $\pm 10\%$.

It calibrates itself to the crystal oscillator at every startup. When the crystal oscillator is switched off, the calibration circuit switches it back on only long enough for a quick calibration (a few milliseconds) to facilitate accurate wake-up timing.

Event Handling

In order to minimize current consumption, the receiver supports the sleep mode. Active mode can be initiated by several wake-up events (wake-up timer timeout, low supply voltage detection, on-chip FIFO filled up or receiving a request through the serial interface).

If any wake-up event occurs, the wake-up logic generates an interrupt signal, which can be used to wake up the microcontroller, effectively reducing the period the microcontroller has to be active. The cause of the interrupt can be read out from the receiver by the microcontroller through the SDO pin.

Interface and Controller

An SPI compatible serial interface lets the user select the frequency band, center frequency of the synthesizer, and the bandwidth of the baseband signal path. Division ratio for the microcontroller clock, wake-up timer period, and low supply voltage detector threshold are also programmable. Any of these auxiliary functions can be disabled when not needed. All parameters are set to default after power-on; the programmed values are retained during sleep mode. The interface supports the read-out of a status register, providing detailed information about the status of the receiver and the received data. It is also possible to store the received data bits into the 16bit RX FIFO register and read them out in a buffered mode. FIFO mode can be enabled through the SPI compatible interface by setting the fe bit to 1 in the Output and FIFO Mode Command.

Standalone Operation Mode

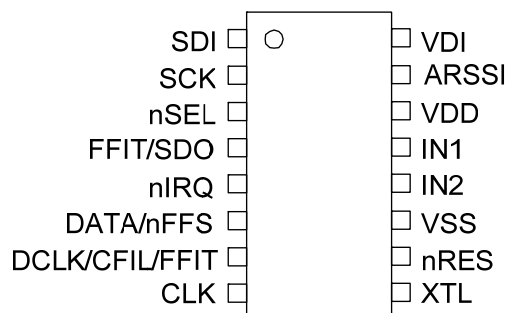
The chip also provides a standalone mode, which allows the use of the receiver without a microcontroller. This mode can be selected by connecting the CLK/LPDM pin to either VDD or VSS. After power on, the chip will check this pin. If it is connected to any supply voltage, then the chip will go to standalone mode. Otherwise, it will go to microcontroller mode and the pin will become an output and provide a clock signal for the microcontroller. To prevent the Si4320 from accidentally entering a standalone mode, the stray capacitance should be kept below 50 pF on pin 8.

In this mode operating parameters can be selected from a limited set by "programming" the receiver over its pins. The chip is addressable and four digital output pins can be controlled by the received data. Selecting the Low Power Duty-Cycle Mode (LPDM) the chip consumes less than 0.5 mA average current.

PACKAGE PIN DEFINITIONS, MICROCONTROLLER MODE

Pin type key: D=digital, A=analog, S=supply, I=input, O=output, IO=input/output

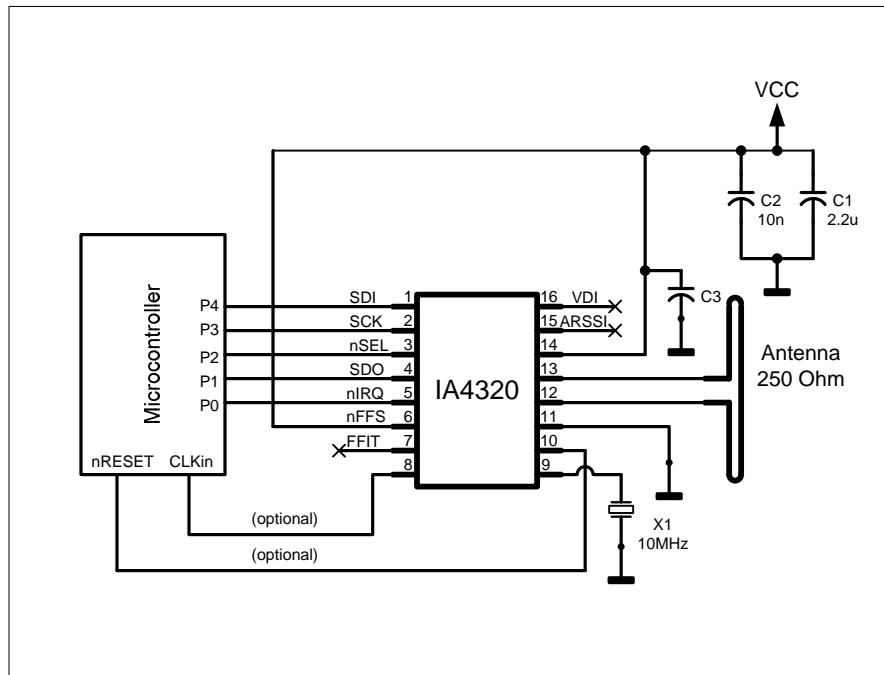
Microcontroller Mode Pin Assignment



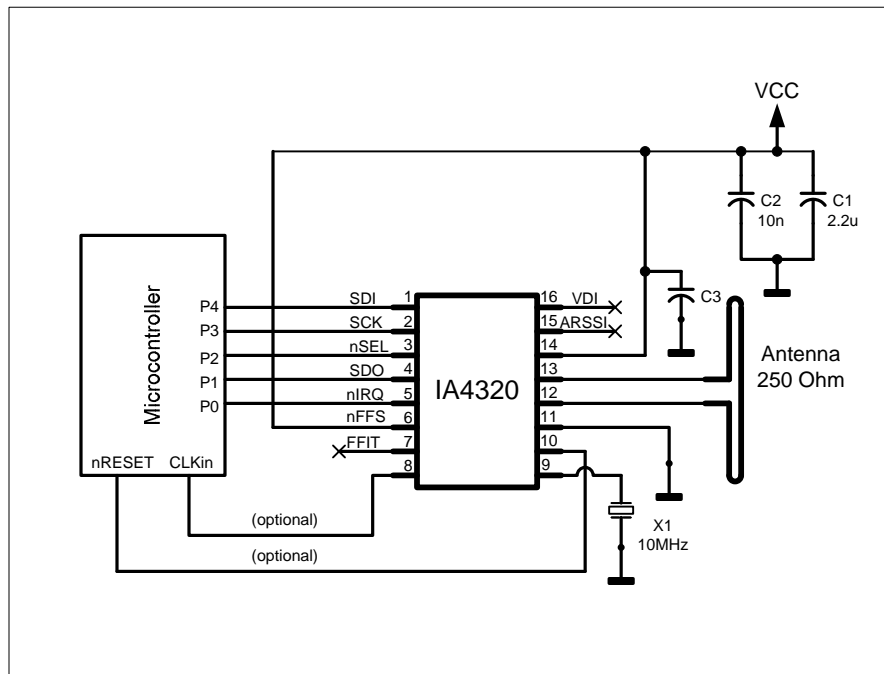
Pin	Name	Type	Function
1	SDI	DI	Data input of serial control interface
2	SCK	DI	Clock input of serial control interface
3	nSEL	DI	Chip select input of three-wire control interface (active low)
4	FFIT/SDO	DO	FIFO IT (active low) or serial data out for Status Read Command. Tristate with bushold cell if nSEL=H
5	nIRQ	DO	Interrupt request output, (active low)
6	DATA	DO	Received data output (FIFO not used)
	nFFS	DI	FIFO select input (active low)
7	DCLK	DO	Received data clock output (Digital filter used, FIFO not used)
	CFIL	AIO	External data filter capacitor connection (Analog filter used)
	FFIT	DO	FIFO IT (active high) FIFO empty function can be achieved when FIFO IT level is set to one
8	CLK	DO	Clock output for the microcontroller
9	XTL/REF	AIO	Crystal connection (other terminal of crystal to VSS) / External reference input
10	nRES	DO	Reset output (active low)
11	VSS	S	Negative supply voltage
12	IN2	AI	RF differential signal input
13	IN1	AI	RF differential signal input
14	VDD	S	Positive supply voltage
15	ARSSI	AO	Analog RSSI output
16	VDI	DO	Valid Data Indicator output

Typical Application, Microcontroller Mode

Minimal Microcontroller Mode



Microcontroller Mode with FIFO usage

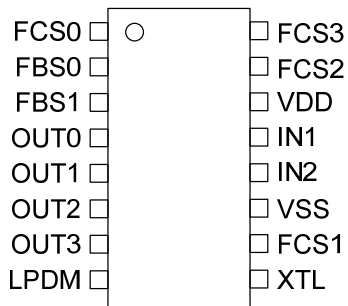


Note: For detailed information about the supply decoupling capacitors see page 7.

PACKAGE PIN DEFINITIONS, STANDALONE MODE

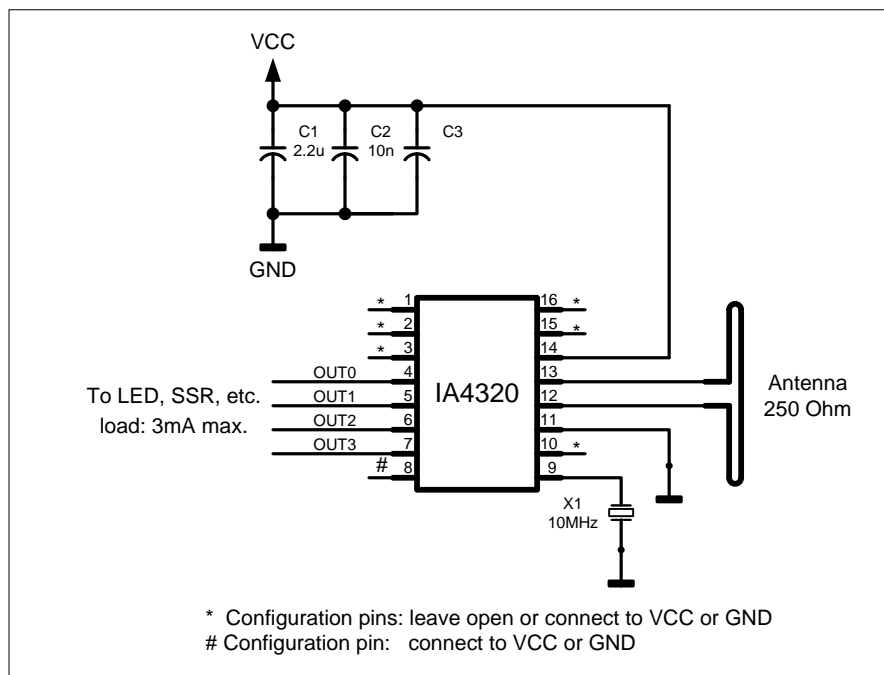
Pin type key: D=digital, A=analog, S=supply, I=input, O=output, IO=input/output

Standalone Mode Pin Assignment



Pin	Name	Type	Function
1	FCS0	DI	Frequency select input bit0
2	FBS0	DI	Band select input bit0
3	FBS1	DI	Band select input bit1
4	OUT0	DO	Control output bit0
5	OUT1	DO	Control output bit1
6	OUT2	DO	Control output bit2
7	OUT3	DO	Control output bit3
8	LPDM	DI	Low power duty cycle mode select input
9	XTL	AIO	Crystal connection (other terminal of crystal to VSS) or external reference input
10	FCS1	DI	Frequency select input bit1
11	VSS	S	Negative supply voltage
12	IN2	AI	RF differential signal input
13	IN1	AI	RF differential signal input
14	VDD	S	Positive supply voltage
15	FCS2	DI	Frequency select input bit2
16	FCS3	DI	Frequency select input bit3

Typical Application, Standalone Mode



Recommended supply decoupling capacitor values

C2 and C3 should be 0603 size ceramic capacitors to achieve the best supply decoupling. The capacitor values are valid for both stand-alone and microcontroller mode.

Band [MHz]	C1	C2	C3
315	2.2 μ F	10nF	390pF
433	2.2 μ F	10nF	220pF
868	2.2 μ F	10nF	47pF
915	2.2 μ F	10nF	33pF

GENERAL DEVICE SPECIFICATIONS

All voltages are referenced to V_{SS} , the potential on the ground reference pin VSS.

Absolute Maximum Ratings (non-operating)

Symbol	Parameter	Min	Max	Units
V_{dd}	Positive supply voltage	-0.5	6.0	V
V_{in}	Voltage on any pin except open collector outputs	-0.5	$V_{dd}+0.5$	V
I_{in}	Input current into any pin except VDD and VSS	-25	25	mA
ESD	Electrostatic discharge with human body model		1000	V
T_{st}	Storage temperature	-55	125	°C
T_{ld}	Lead temperature (soldering, max 10 s)		260	°C

Recommended Operating Range

Symbol	Parameter	Min	Max	Units
V_{dd}	Positive supply voltage	2.2	5.4	V
T_{op}	Ambient operating temperature	-40	85	°C

ELECTRICAL SPECIFICATION

(Test Conditions: $T_{op} = 27\text{ °C}$; $V_{dd} = V_{oc} = 3.3\text{ V}$)

DC Characteristics

Symbol	Parameter	Conditions/Notes	Min	Typ	Max	Units
I_{dd}	Supply current	315 / 433 MHz bands		9	11	mA
		868 MHz band		10.5	12.5	
		915 MHz band		12	14	
I_{pd}	Standby current	All blocks disabled		0.3		μA
I_{lb}	Low battery voltage detector current consumption			0.5		μA
I_{wt}	Wake-up timer current consumption (Note 1)			1.5		μA
I_x	Idle current	Crystal oscillator and base band parts are ON		3.0	3.5	mA
V_{lb}	Low battery detect threshold	Programmable in 0.1 V steps	2.25		5.35	V
V_{lba}	Low battery detection accuracy			+/-3		%
V_{il}	Digital input low level				$0.3 \cdot V_{dd}$	V
V_{ih}	Digital input high level		$0.7 \cdot V_{dd}$			V
I_{il}	Digital input current	$V_{il} = 0\text{ V}$	-1		1	μA
I_{ih}	Digital input current	$V_{ih} = V_{dd}$, $V_{dd} = 5.4\text{ V}$	-1		1	μA
V_{ol}	Digital output low level	$I_{ol} = 2\text{ mA}$			0.4	V
V_{oh}	Digital output high level	$I_{oh} = -2\text{ mA}$	$V_{dd}-0.4$			V

Note 1: Using the internal wake-up timer and counter reduces the overall current consumption, which should permit approximately 6 months operation from a 1500mAh battery.

AC Characteristics

Symbol	Parameter	Conditions/Notes	Min	Typ	Max	Units
f_{LO}	Receiver frequency	315 MHz band, 2.5 kHz resolution	310.24		319.75	MHz
		433 MHz band, 2.5 kHz resolution	430.24		439.75	
		868 MHz band, 5.0 kHz resolution	860.48		879.51	
		915 MHz band, 7.5 kHz resolution	900.72		929.27	
BW	Base-band bandwidth	mode 0	60	67	75	kHz
		mode 1	120	134	150	
		mode 2	180	200	225	
		mode 3	240	270	300	
		mode 4	300	350	375	
		mode 5	360	400	450	
BR	FSK bit rate	With internal digital filters			115.2	kbps
BRA	FSK bit rate	With analog filter			256	kbps
P_{min}	Receiver Sensitivity	BER 10^{-3} , BW=67 kHz, BR=1.2 kbps (Note 1)		-109	-100	dBm
AFC _{range}	AFC locking range	δf_{FSK} : FSK deviation in the received signal		$0.8 \cdot \delta f_{FSK}$		
IIP3 _{inh}	Input IP3	In band interferers in high bands		-21		dBm
IIP3 _{outh}	Input IP3	Out of band interferers $f - f_{LO} > 4\text{MHz}$		-18		dBm
IIP3 _{inl}	IIP3 (LNA –6dB gain)	In band interferers in low bands		-15		dBm
IIP3 _{outl}	IIP3 (LNA –6dB gain)	Out of band interferers $f - f_{LO} > 4\text{MHz}$		-12		dBm
P_{max}	Maximum input power	LNA: high gain	0			dBm
Rin	RF input impedance real part (differential) (Note 2)	LNA gain (0, -14dB) LNA gain (-6, -20dB)		250 500		Ohm
Cin	RF input capacitance			1		pF
RS _a	RSSI accuracy			+/-5		dB
RS _r	RSSI range			46		dB
C _{ARSSI}	Filter cap for ARSSI		1			nF
RS _{step}	RSSI programmable level steps			6		dB
RS _{resp}	DRSSI response time	Until the RSS output goes high after the input signal exceeds the preprogrammed limit C _{ARSSI} =5nF		500		μs

Note 1: See the BER diagrams in the measurement results section for detailed information.

Note 2: See matching circuit parameters and antenna design guide for information, and Application Notes available from www.silabs.com/integration.

AC Characteristics (continued)

Symbol	Parameter	Conditions/Notes	Min	Typ	Max	Units
f_{ref}	PLL reference frequency	(Note 3)	8	10	12	MHz
f_{res}	PLL frequency resolution	Depends on selected bands	2.5		7.5	kHz
t_{lock}	PLL lock time	Frequency error < 1kHz after 10 MHz step		20		μ s
$t_{st, P}$	PLL startup time	With running crystal oscillator			250	μ s
C_{xl}	Crystal load capacitance, see crystal selection guide	Programmable in 0.5 pF steps, tolerance +/- 10%	8.5		16	pF
t_{POR}	Internal POR pulse width (Note 4)	After V_{dd} has reached 90% of final value		50	150	ms
t_{sx}	Crystal oscillator startup time	Crystal ESR < 100 Ohms (Note 5)		1	5	ms
t_{PBT}	Wake-up timer accuracy	Crystal oscillator must be enabled to ensure proper calibration at startup (Note 5)		+/-10		%
$t_{wake-up}$	Programmable wake-up time		1		$5 \cdot 10^{11}$	ms
$C_{in, D}$	Digital input capacitance				2	pF
$t_{r, f}$	Digital output rise/fall time	15 pF pure capacitive load			10	ns

Note 3: Using other than a 10 MHz crystal is not recommended because the crystal referred timing and frequency parameters will change accordingly.

Note 4: During this period, commands are not accepted by the chip. For detailed information see the *Reset modes* section.

Note 5: The crystal oscillator start-up time strongly depends on the capacitance seen by the oscillator. Using low capacitance and low ESR crystal is recommended. When designing the PCB layout keep the trace connecting to the crystal short to minimize stray capacitance.

CONTROL INTERFACE

Commands to the receiver are sent serially. Data bits on pin SDI are shifted into the device upon the rising edge of the clock on pin SCK whenever the chip select pin nSEL is low. When the nSEL signal is high, it initializes the serial interface. The number of bits sent is an integer multiple of 8. All commands consist of a command code, followed by a varying number of parameter or data bits. All data are sent MSB first (e.g. bit 15 for a 16-bit command). Bits having no influence (don't care) are indicated with X. The Power On Reset (POR) circuit sets default values in all control registers.

The status information or received data can be read serially over the SDO pin. Bits are shifted out upon the falling edge of CLK signal. When the nSEL is high, the SDO output is in a high impedance state.

The receiver will generate an interrupt request (IRQ) for the microcontroller on the following events:

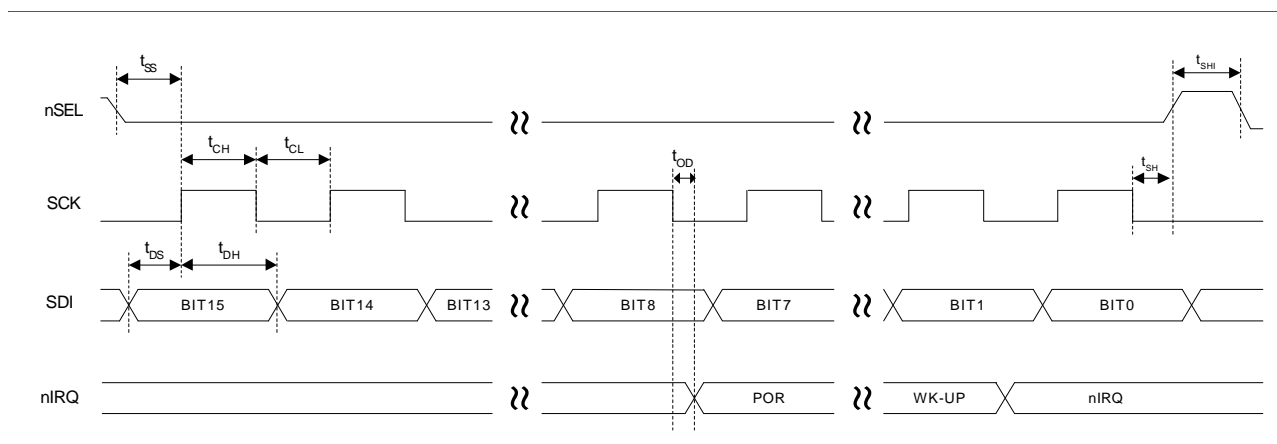
- Supply voltage below the preprogrammed value is detected (LBD)
- Wake-up timer timeout (WK-UP)
- FIFO received the preprogrammed amount of bits (FFIT)
- FIFO overflow (FFOV)

FFIT and FFOV are applicable only when the FIFO is enabled. To find out why the nIRQ was issued, the status bits should be read out.

Timing Specification

Symbol	Parameter	Minimum value [ns]
t_{CH}	Clock high time	25
t_{CL}	Clock low time	25
t_{SS}	Select setup time (nSEL falling edge to SCK rising edge)	10
t_{SH}	Select hold time (SCK falling edge to nSEL rising edge)	10
t_{SHI}	Select high time	25
t_{DS}	Data setup time (SDI transition to SCK rising edge)	5
t_{DH}	Data hold time (SCK rising edge to SDI transition)	5
t_{OD}	Data delay time	10

Timing Diagram



Control Commands

	Control Word	Related Parameters/Functions	Related Control Bits
1	Configuration Setting Command	Frequency band, low battery detector, wake-up timer, crystal oscillator load capacitance, baseband filter bandwidth, clock output	b1 to b0, eb, et, ex, x3 to x0, i2 to i0, dc
2	Frequency Setting Command	Set the frequency of the local oscillator	f11 to f0
3	Receiver Setting Command	Set VDI source, LNA gain, RSSI threshold,	d1 to d0, g1 to g0, r2 to r0, en
4	Wake-up Timer Command	Wake-up time period	r4 to r0, m7 to m0
5	Low Duty-Cycle Command	Set duty-cycle, enable low duty-cycle mode.	d6 to d0, en
6	Low Battery Detector and Clock Divider Command	Set LBD threshold voltage and microcontroller clock division ratio	d2 to d0, t4 to t0
7	AFC Control Command	Set AFC parameters	a1 to a0, r11 to r10, st, fi, oe, en
8	Data Filter Command	Set data filter type, clock recovery parameters	al, ml, s1 to s0, f2 to f0
9	Data Rate Command	Bit rate	cs, r6 to r0
10	Output and FIFO Command	Set FIFO IT level, FIFO start control, FIFO enable and FIFO fill enable	f3 to f0, s1 to s0, ff, fe
11	Reset Mode Command	Enable / disable sensitive reset	dr
12	Status Read Command	Read status information	

Note: In the following tables the POR column shows the default values of the command registers after power-on.

1. Configuration Setting Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	0	b1	b0	eb	et	ex	x3	x2	x1	x0	i2	i1	i0	dc	893Ah

b1	b0	Frequency Band [MHz]
0	0	315
0	1	433
1	0	868
1	1	915

i2	i1	i0	Baseband Bandwidth [kHz]
0	0	0	reserved
0	0	1	400
0	1	0	340
0	1	1	270
1	0	0	200
1	0	1	134
1	1	0	67
1	1	1	reserved

x3	x2	x1	x0	Crystal Load Capacitance [pF]
0	0	0	0	8.5
0	0	0	1	9.0
0	0	1	0	9.5
0	0	1	1	10.0
...				
1	1	1	0	15.5
1	1	1	1	16.0

Bits *eb* and *et* control the operation of the low battery detector and wake-up timer, respectively. They are enabled when the corresponding bit is set.

If *ex* is set the crystal is active during sleep mode. When *dc* bit is set it disables the clock output

2. Frequency Setting Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	1	0	f11	f10	f9	f8	f7	f6	f5	f4	f3	f2	f1	f0	A680h

The 12-bit parameter of the *Frequency Setting Command* <f11 : f0> has the value F. The value F should be in the range of 96 and 3903. When F is out of range, the previous value is kept. The synthesizer center frequency f_0 can be calculated as:

$$f_0 = 10 \text{ MHz} * C1 * (C2 + F/4000)$$

The constants C1 and C2 are determined by the selected band as:

Band [MHz]	C1	C2
315	1	31
433	1	43
868	2	43
915	3	30

3. Receiver Setting Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	0	0	0	d1	d0	g1	g0	r2	r1	r0	en	C0C1h

Bits 7-6 select the VDI (valid data indicator) signal:

d1	d0	VDI output
0	0	Digital RSSI Out (DRSSI)
0	1	Data Quality Detector Output (DQD)
1	0	Clock recovery lock
1	1	DRSSI && DQD

Bits 5-4 LNA gain set:

g1	g0	G _{LNA} (dB relative to max. G)
0	0	0
0	1	-14
1	0	-6
1	1	-20

Bits 3-1 control the threshold of the RSSI detector:

r2	r1	r0	RSSI _{setth} [dBm]
0	0	0	-103
0	0	1	-97
0	1	0	-91
0	1	1	-85
1	0	0	-79
1	0	1	-73
1	1	0	Reserved
1	1	1	Reserved

The RSSI threshold depends on the LNA gain, the real RSSI threshold can be calculated:

$$\text{RSSI}_{\text{th}} = \text{RSSI}_{\text{setth}} + G_{\text{LNA}}$$

Bit 0 (en) enables the whole receiver chain when set. Enable/disable of the wake-up timer and the low battery detector are not affected by this setting.

Note: Clock tail is not generated when the crystal oscillator is controlled by en bit.

4. Wake-Up Timer Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	1	r4	r3	r2	r1	r0	m7	m6	m5	m4	m3	m2	m1	m0	E196h

The wake-up time period can be calculated by M <m7 : m0> and R <r4 : r0>:

$$T_{\text{wake-up}} = M * 2^R \text{ ms}$$

Software reset: Sending FF00h command to the chip triggers software reset. For more details see the *Reset modes* section.

5. Low Duty-Cycle Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	1	0	0	d6	d5	d4	d3	d2	d1	d0	en	CC0Eh

With this command Low Duty-Cycle operation can be set in order to decrease the average power consumption.

The time cycle is determined by the *Wake-Up Timer Command*.

The Duty-Cycle is calculated by D <d6 : d0> and M. (M is parameter in a *Wake-Up Timer Command*.)

$$\text{D.C.} = (D * 2 + 1) / M * 100\%$$

6. Low Battery Detector and Microcontroller Clock Divider Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	0	1	0	d2	d1	d0	t4	t3	t2	t1	t0	C200h

The 5-bit value T of t4-t0 determines the threshold voltage of the threshold voltage V_{th} of the detector:

$$V_{\text{th}} = 2.25 \text{ V} + T * 0.1 \text{ V}$$

Clock divider configuration:

d2	d1	d0	Clock Output Frequency [MHz]
0	0	0	1
0	0	1	1.25
0	1	0	1.66
0	1	1	2
1	0	0	2.5
1	0	1	3.33
1	1	0	5
1	1	1	10

7. AFC Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	1	1	0	a1	a0	r11	r10	st	fi	oe	en	C6F7h

Bit 0 (*en*) enables the calculation of the offset frequency by the AFC circuit (it allows the addition of the content of the output register to the frequency control word of the PLL).

Bit 1 (*oe*) when set, enables the output (frequency offset) register

Bit 2 (*fi*) when set, switches the circuit to high accuracy (fine) mode. In this case the processing time is about four times longer, but the measurement uncertainty is less than half.

Bit 3 (*st*) strobe edge, when *st* goes to high, the actual latest calculated frequency error is stored into the output registers of the AFC block.

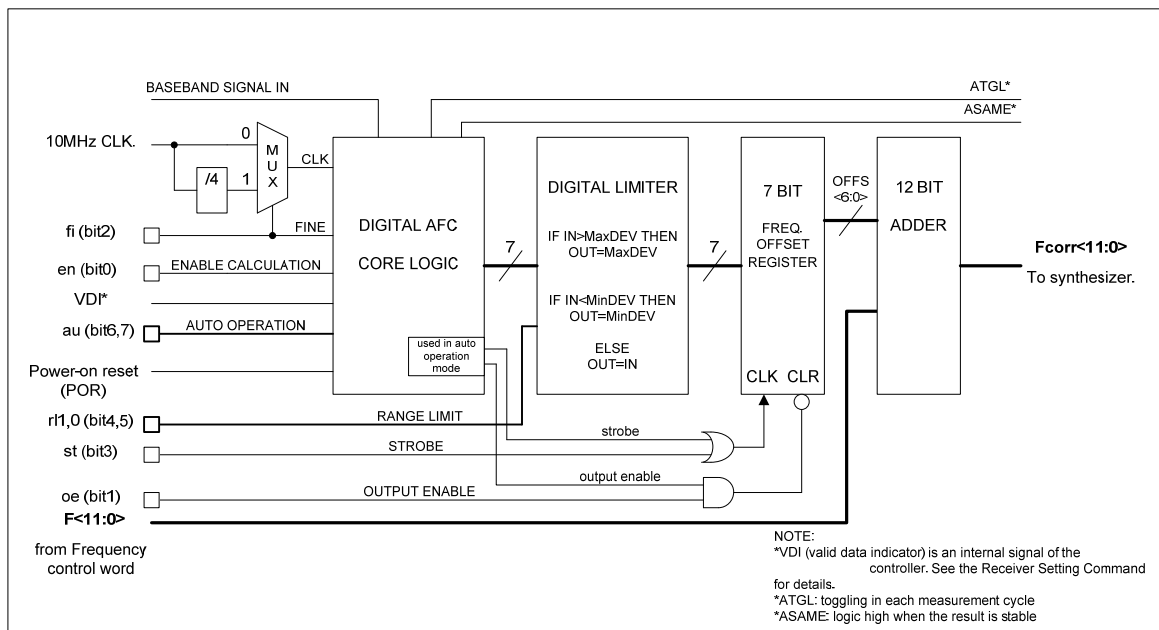
Bit 4-5 (*r10*, *r11*) range limit: Limits the value of the frequency offset register to the following values:

r11	r10	Max dev [f_{res}]
0	0	No restriction
0	1	+15/-16
1	0	+7/-8
1	1	+3/-4

f_{res} :
 315, 433MHz bands: 2.5kHz
 868MHz band: 5kHz
 915MHz band: 7.5kHz

Bit 6-7 (*a0*, *a1*) Automatic operation mode selector:

a1	a0	Automatic operation mode
0	0	Auto mode off (Strobe is controlled by microcontroller)
0	1	Runs only once after each power-up
1	0	Drop the f_{offset} value when the VDI signal is low
1	1	Keep the f_{offset} value independently from the state of the VDI signal



In automatic operation mode (no strobe signal is needed from the microcontroller to update the output offset register), the AFC circuit is automatically enabled when VDI indicates a potential incoming signal during the whole measurement cycle and the circuit measures the same result in two subsequent cycles.

There are three operation modes, example from the possible application:

1, ($a1=0$, $a0=1$) The circuit measures the frequency offset only once after power up. This way, the extended TX/RX maximum distance can be achieved. Possible usage: In the final application when the user is inserted the battery the circuit measures and compensate the frequency offset caused by the crystal tolerances. This method enables to use cheaper quartz in the application and provide quite good protection against locking in an interferer.

2a, ($a1=1$, $a0=0$) The circuit measures automatically the frequency offset during an initial low data rate pattern –easier to receive- (i.e.: 00110011) of the package and change the receiving frequency according that. The further part of the package can be received by the corrected frequency settings.

2b, ($a1=1$, $a0=0$) The transmitter must transmit the first part of the packet with a step higher deviation and later there is a possibility to reduce it.

In both cases (2a and 2b) when the VDI indicates poor receiving conditions (VDI goes low) the output register is automatically cleared. It's suggested to use when one receiver receives signal from more than one transmitter.

3, ($a1=1$, $a0=1$) It is similar to the 2a and 2b modes, but 3 is suggested to use when a receiver operates with only one transmitter. After a complete measuring cycle, the measured value is held independently of the state of VDI signal.

8. Data Filter Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	1	1	0	0	0	1	0	0	al	ml	1	s1	s0	f2	f1	f0	POR C42Ch

Bit 7 <al>: Clock recovery (CR) auto lock control if set.

It means that the CR start in fast mode after locking it automatically switches to slow mode.

Bit 6 <ml>: Clock recovery lock control

1: fast mode, fast attack and fast release

0: slow mode, slow attack and slow release

Using the slower one requires more accurate bit timing (see Data Rate Command).

Bit 3-4 <s0 : s1>: Select the type of the data filter:

s1	s0	Filter Type
0	0	OOK to filter
0	1	Digital filter
1	0	Reserved
1	1	Analog RC filter

OOK to filter: the analog RSSI signal is used as received data. The DRSSI threshold level is used for slicing.

Digital: this is a digital realization of an analog RC filter followed by a comparator with hysteresis. The time constant is automatically adjusted to the bit rate defined by the Data Rate Command.

Analog RC filter: The demodulator output is fed to pin 7 over a 10 kOhm resistor. The filter cut-off frequency is set by the external capacitor connected to this pin and VSS.

The table shows the optimal filter capacitor values for different data rates:

1.2 kbps	2.4 kbps	4.8 kbps	9.6 kbps	19.2 kbps	38.4 kbps	57.6 kbps	115.2 kbps	256 kbps
12 nF	8.2 nF	6.8 nF	3.3 nF	1.5 nF	680 pF	270 pF	150 pF	100 pF

Note: If analog RC filter is selected the internal clock recovery circuit and the FIFO cannot be used.

Bit 0-2 <f0 : f2>: DQD threshold parameter.

Note: To let the DQD report "good signal quality" the threshold parameter should be less than 4 in the case when the bitrate is close to the deviation. At higher deviation/bitrate settings higher threshold parameter can report "good signal quality" as well.

9. Data Rate Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	0	0	0	cs	r6	r5	r4	r3	r2	r1	r0	C823h

The expected bit rate of the received data stream is determined by the 7-bit value R (bits r6 to r0) and the 1 bit cs.

$$BR = 10 \text{ MHz} / 29 / (R+1) / (1 + cs*7)$$

In the receiver set R according the next function:

$$R = (10 \text{ MHz} / 29 / (1 + cs*7) / BR) - 1$$

Apart from setting custom values, the standard bit rates from 600 bps to 115.2 kbps can be approximated with small error.

Data rate accuracy requirements:

$$\text{Clock recovery in slow mode: } \Delta BR / BR < 1 / (29 * N_{\text{bit}})$$

$$\text{Clock recovery in fast mode: } \Delta BR / BR < 3 / (29 * N_{\text{bit}})$$

BR is the bit rate set in the receiver and ΔBR is bit rate difference between the transmitter and the receiver. N_{bit} is the maximal number of consecutive ones or zeros in the data stream. It is recommended for long data packets to include enough 1/0 and 0/1 transitions, and be careful to use the same division ratio in the receiver and in the transmitter.

ΔBR is a theoretical limit for the clock recovery circuit. Clock recovery will not work above this limit. The clock recovery circuit will always operate below this limit independently from process, temperature, or V_{dd} condition.

Supposing a maximum length of consecutive zeros or ones in the data stream is less than 5 bits, the necessary relative accuracy is 0.68% in slow mode and 2.1% in fast mode.

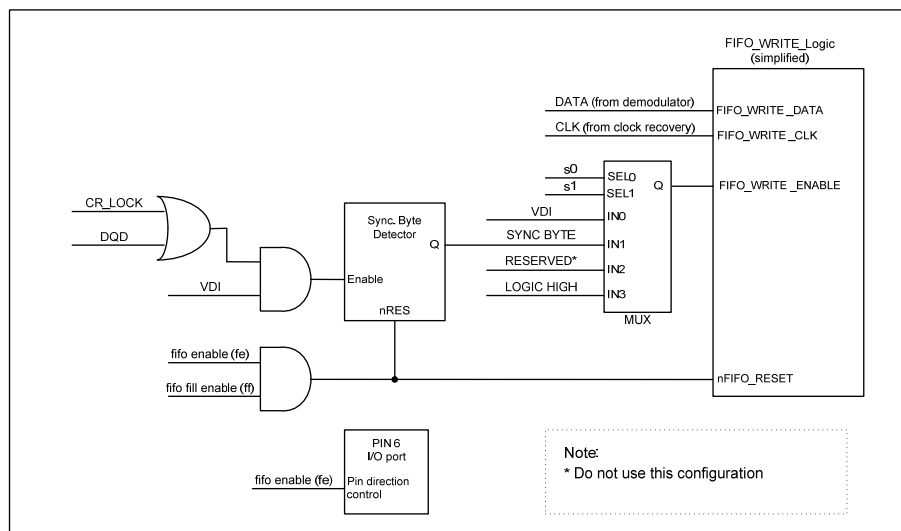
10. Output and FIFO Mode Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	1	1	0	f3	f2	f1	f0	s1	s0	ff	fe	CE85h

Bit 4-7 <f3 : f0>: FIFO IT level. The FIFO generates IT when number of the received data bits reaches this level.

Bit 2-3 <s1 : s0>: Set the input of the FIFO fill start condition:

s1	s0	FIFO fill start condition
0	0	VDI
0	1	Sync Word
1	0	Reserved
1	1	Always



Note: VDI (Valid Data Indicator) see further details in *Receiver Control Word*, Synchron word in microcontroller mode is 2DD4h.

Bit 1: <ff> Enables FIFO fill after synchron word reception. FIFO fill stops when this bit is cleared.

Bit 0: <fe> Enables the 16bit deep FIFO mode. To clear the FIFO's counter and content, it has to be set zero.

Note: To restart the synchron word reception, bit 1 should be cleared and set. This action will initialize the FIFO and clear its content.

Bit 0 modifies the function of pin 6 and pin 7. Pin 6 (nFFS) will become input if fe is set to 1. If the chip is used in FIFO mode, do not allow this to be a floating input.

11. Reset Mode Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	1	1	0	1	0	0	0	0	0	0	0	0	dr	DA00h

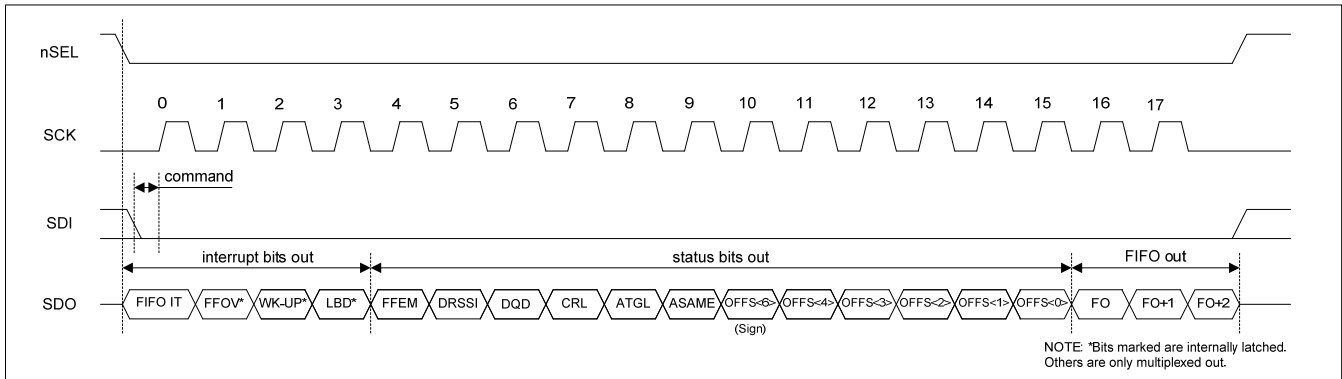
Bit 0 (dr): Disables the highly sensitive RESET mode. If this bit is cleared, a 600 mV glitch in the power supply may cause a system reset. For more detailed description see the *Reset modes* section.

12. Status Read Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	--

The read command starts with a zero, whereas all other control commands start with a one. Therefore, after receiving the first bit of the control command the Si4320 identifies it as a read command. So as the first bit of the command is received, the receiver starts to clock out the status bits on the SDO output as follows:

Status Register Read Sequence with FIFO Read Example



It is possible to read out the content of the FIFO after the reading of the status bits. The command can be aborted after any read bits by rising edge of the select signal.

Note: The FIFO IT bit behaves like a status bit, but generates nIRQ pulse if active. To check whether there is a sufficient amount of data in the FIFO, the SDO output can be tested. In extreme speed critical applications, it can be useful to read only the first four bits (FIFO IT - LBD) to clear the FFOV, WK-UP, and LBD bits. During the FIFO access the f_{SCK} cannot be higher than $f_{ref}/4$, where f_{ref} is the crystal oscillator frequency. If the FIFO is read in this mode the nFFS input must be connected to logic high level.

Definitions of the bits in the above timing diagram:

FIFO IT	Number of the data bits in the FIFO is reached the preprogrammed limit
FFOV	FIFO overflow
WK-UP	Wake-up timer overflow
LBD	Low battery detect, the power supply voltage is below the preprogrammed limit
FFEM	FIFO is empty
DRSSI	The strength of the incoming signal is above the preprogrammed limit
DQD	Data Quality Detector detected a good quality signal
CRL	Clock recovery lock
ATGL	Toggling in each AFC cycle
ASAME	AFC stabilized (measured twice the same offset value)
OFFS6, 4-0	Offset value to be added to the value of the Frequency control word

FIFO Buffered Data Read

In this operating mode, incoming data are clocked into a 16 bit FIFO buffer. The receiver starts to fill up the FIFO when the Valid Data Indicator (VDI) bit and/or the synchron word recognition circuit indicates potentially real incoming data. This prevents the FIFO from being filled with noise and overloading the external microcontroller.

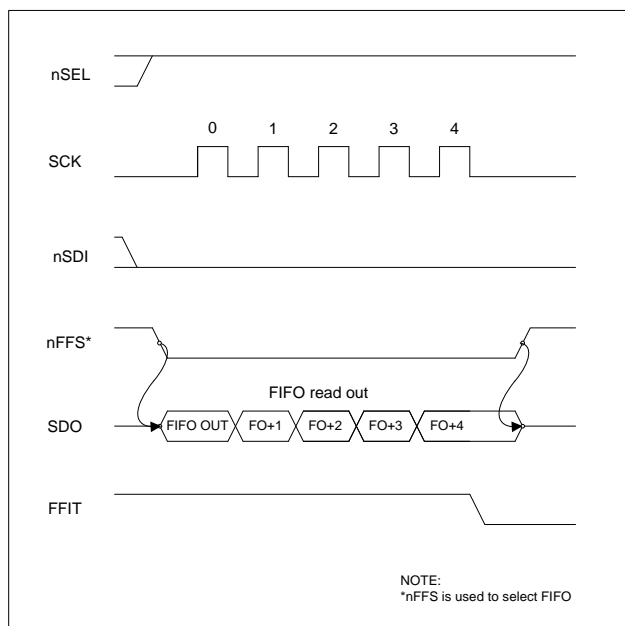
For further details see the *Receiver Setting Command* and the *Output and FIFO Command*.

Polling Mode:

The nFFS signal selects the buffer directly and its content could be clocked out through pin SDO by SCK. Set the FIFO IT level to 1. In this case, as long as FFIT indicates received bits in the FIFO, the controller may continue to take the bits away. When FFIT goes low, no more bits need to be taken. An SPI read command is also available.

Interrupt Controlled Mode:

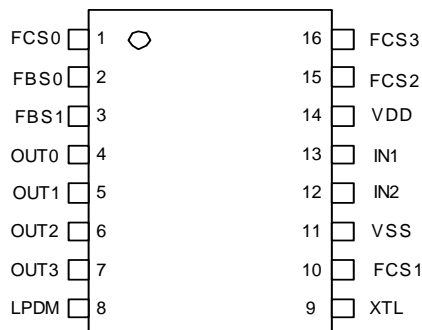
The user can define the FIFO level (the number of received bits) which will generate the nFFIT when exceeded. The status bits report the changed FIFO status in this case.



During FIFO access the f_{SCK} cannot be higher than $f_{ref}/4$, where f_{ref} is the crystal oscillator frequency.

STANDALONE OPERATION

The chip supports standalone operation, meaning that with preprogrammed (hard wired) parameters, a simple receiver can be built without an external microcontroller. After the power-up sequence, the status of pin 8 is queried by connecting internally about 10 μ A current on it. If VSS or VDD is detected, the chip turns to standalone mode. In this case 7 pins are used to configure the receiver and 4 digital outputs are available:



In the standalone mode, a predefined data sequence should be employed which contains preamble, synchron, chip address, and function control bytes. To allow the control of the outputs, the chip should receive its chip address byte and twice the same function control byte.

The required data flow sequence:

Preamble Byte	Synchron Byte	Chip Address Byte	Function Control Byte	One's complement of Function Control Byte	Function Control Byte
AAh	2Dh	D4h D2h B4h B2h	See below	See below	See below

As a minimum preamble, use at least 16 bits.

The structure of the Function Control Byte is shown below. For each output there are two bits assigned to define their mode of operation:

OUT3 F1	OUT3 F0	OUT2 F1	OUT2 F0	OUT1 F1	OUT1 F0	OUT0 F1	OUT0 F0
------------	------------	------------	------------	------------	------------	------------	------------

OUT3 / F1 sent out first., OUT0 – OUT3 represent the four digital output pins, F0 - F1 represents the function bits.

Output functions controlled by the function bits, as follows:

F1	F0	Function
0	0	No change
0	1	Sets output logical low
1	0	Sets output logical high
1	1	Sets output high in mono-stable mode, cycle time is 100 ms

Mono-stable mode will be restarted as long as the proper *Function Control Byte* is received.

The following receiving frequencies can be set with the different static external pin settings:

PIN16 FCS3	PIN15 FCS2	PIN10 FCS1	PIN1 FCS0	F _{receiving} PIN2=0 PIN3=0	F _{receiving} PIN2=1 PIN3=0	F _{receiving} PIN2=0 PIN3=1	F _{receiving} PIN2=1 PIN3=1	Chip Address Byte
0	0	0	0	310.320	433.360	(867.680)	(900.960)	D4h
0	0	0	Z or 1	310.960	433.440	(867.840)	902.880	D2h
0	0	Z	0	311.600	433.520	(868.000)	904.800	B4h
0	0	Z	Z or 1	312.240	433.600	868.160	906.720	B2h
0	Z	0	0	312.880	433.680	868.320	908.640	D4h
0	Z	0	Z or 1	313.520	433.760	868.480	910.560	D2h
0	Z	Z	0	314.160	433.840	868.640	912.480	B4h
0	Z	Z	Z or 1	314.800	433.920	868.800	914.400	B2h
Z	0	0	0	315.440	434.000	868.960	916.320	D4h
Z	0	0	Z or 1	316.080	434.080	869.120	918.240	D2h
Z	0	Z	0	316.720	434.160	869.280	920.160	B4h
Z	0	Z	Z or 1	317.360	434.240	869.440	922.080	B2h
Z	Z	0	0	318.000	434.320	869.600	924.000	D4h
Z	Z	0	Z or 1	318.640	434.400	869.760	925.920	D2h
Z	Z	Z	0	319.280	434.480	869.920	927.840	B4h
Z	Z	Z	Z or 1	319.920	434.560	(870.080)	(929.760)	B2h

Note 1: Z: Not connected (floating) pin

Note 2: Values shown as *(italic)* are out-of-band frequencies.

Note 3: If FCS0=1 (connected to VDD) the RSSI threshold limit is changed from -103 dBm to -97 dBm.

Note 4: In standalone mode, the operation parameters related to the band, frequency selection and chip address are determined by the table above. All other control bits (filter bandwidth, bit rate etc.) are determined by the power-on values of the different control registers.

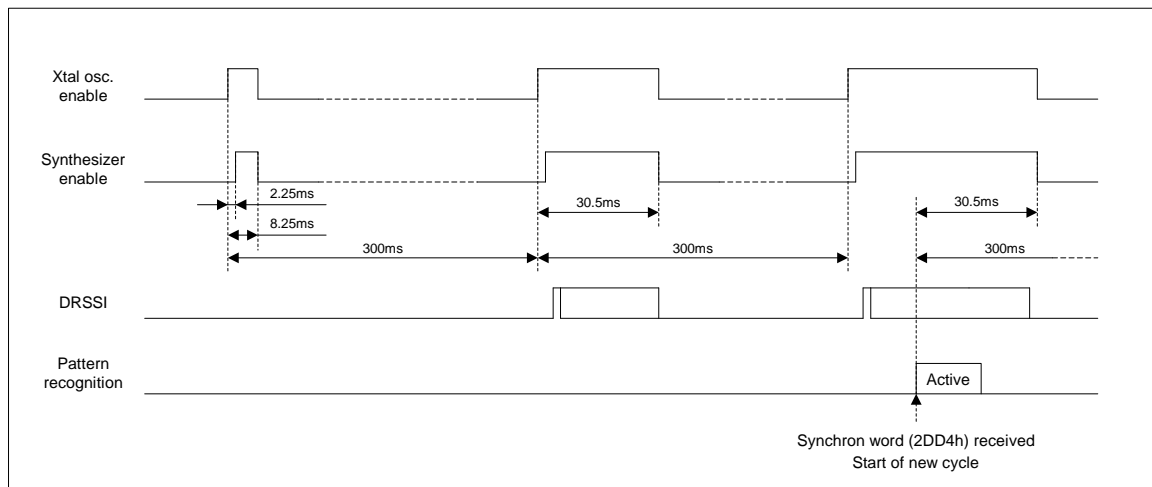
Note 5: It is possible to use the receiver in a so-called "mixed mode". The SPI bus architecture allows access to the bus in standalone mode (pins 1, 2, 3) and thereby makes it possible to overwrite the default POR values of the control registers. In this way the operating parameters of the receiver can be programmed over the interface while performing the functions of the standalone mode when receiving the proper data sequence.

Low Power Duty-Cycle Operation (LPDM)

To use this mode, pin 8 must be connected to VDD. The logic value of pin 8 defines whether the receiver works in *Low Power Duty-Cycle Mode* (LPDM) or not. If the value is high (VDD detected), the chip will wake up in every 300 ms. If the value is low (GND detected), then the chip is continually ON (active). The chip uses the internal wake-up timer and counter for timing the on/off process. This method reduces the overall current consumption, which should permit approximately 6 months operation from a 1500 mAh battery.

Low Power Duty-Cycle Internal Operations and Timings (Wake-up on Radio)

The wake-up timer event switches on the crystal oscillator, the internal logic waits about 2.25ms. When the oscillator is stable the controller switches on the synthesizer as well. The receiver monitors the incoming signal strength during this "ON" state of LPDM. If in the next 6ms the incoming signal strength is above the defined limit (-103dBm if FCS0=0 or -97dBm if FCS0=1), the synthesizer remains switched on for 30.5ms, otherwise it switches itself off after the 6ms operation time. The period time is about 300ms.



Note 1: Every detected synchron word restarts the timer, which controls the 'ON' state of the receiver.

Note 2: If the internal *Pattern Recognition* block is active (decoding the synchron word), then the internal logic does not switch the synthesizer off until the incoming data is fully processed.

RX-TX ALIGNMENT PROCEDURES

RX-TX frequency offset can be caused only by the differences in the actual reference frequency. To minimize these errors it is suggested to use the same crystal type and the same PCB layout for the crystal placement on the RX and TX PCBs.

To verify the possible RX-TX offset it is suggested to measure the CLK output of both chips with a high level of accuracy. Do not measure the output at the XTL pin since the measurement process itself will change the reference frequency. Since the carrier frequencies are derived from the reference frequency, having identical reference frequencies and nominal frequency settings at the TX and RX side there should be no offset if the CLK signals have identical frequencies.

It is possible to monitor the actual RX-TX offset using the AFC status report included in the status byte of the receiver. By reading out the status byte from the receiver, the actual measured offset frequency will be reported. In order to get accurate values the AFC has to be disabled during the read by clearing the "en" bit in the AFC Control Command (bit 0).

CRYSTAL SELECTION GUIDELINES

The crystal oscillator of the Si4320 requires a 10 MHz parallel mode crystal. The circuit contains an integrated load capacitor in order to minimize the external component count. The internal load capacitance value is programmable from 8.5 pF to 16 pF in 0.5 pF steps. With appropriate PCB layout, the total load capacitance value can be 10 pF to 20 pF so a variety of crystal types can be used.

When the total load capacitance is not more than 20 pF and a worst case 7 pF shunt capacitance (C_0) value is expected for the crystal, the oscillator is able to start up with any crystal having less than 300 ohms ESR (equivalent series loss resistance). However, lower C_0 and ESR values guarantee faster oscillator startup.

The crystal frequency is used as the reference of the PLL, which generates the local oscillator frequency (f_{LO}). Therefore, f_{LO} is directly proportional to the crystal frequency. The accuracy requirements for production tolerance, temperature drift and aging can thus be determined from the maximum allowable local oscillator frequency error.

Maximum XTAL Tolerances Including Temperature and Aging [ppm]

Bit Rate: 2.4kbps	Transmitter Deviation [± kHz]						
	30	60	90	120	150	180	210
315 MHz	30	75	100	100	100	100	100
433 MHz	20	50	75	100	100	100	100
868 MHz	10	25	40	60	75	100	100
915 MHz	10	25	40	50	75	75	100

Bit Rate: 9.6kbps	Transmitter Deviation [± kHz]						
	30	60	90	120	150	180	210
315 MHz	25	70	100	100	100	100	100
433 MHz	15	50	75	100	100	100	100
868 MHz	8	25	40	60	75	75	100
915 MHz	8	25	40	50	70	75	100

Bit Rate: 38.3kbps	Transmitter Deviation [± kHz]						
	30	60	90	120	150	180	210
315 MHz	don't use	30	75	100	100	100	100
433 MHz	don't use	20	50	75	100	100	100
868 MHz	don't use	10	30	40	60	75	100
915 MHz	don't use	10	25	40	60	75	75

Whenever a low frequency error is essential for the application, it is possible to “pull” the crystal to the accurate frequency by changing the load capacitor value. The widest pulling range can be achieved if the nominal required load capacitance of the crystal is in the “midrange”, for example 16 pF. The “pull-ability” of the crystal is defined by its motional capacitance and C_0 .

The on chip AFC is capable to correct TX/RX carrier offsets as much as 80% of the deviation of the received FSK modulated signal.

Note: There may be other requirements for the TX carrier accuracy with regards to the requirements as defined by standards and/or channel separations.

RESET MODES

The chip will enter into reset mode if any of the following conditions are met:

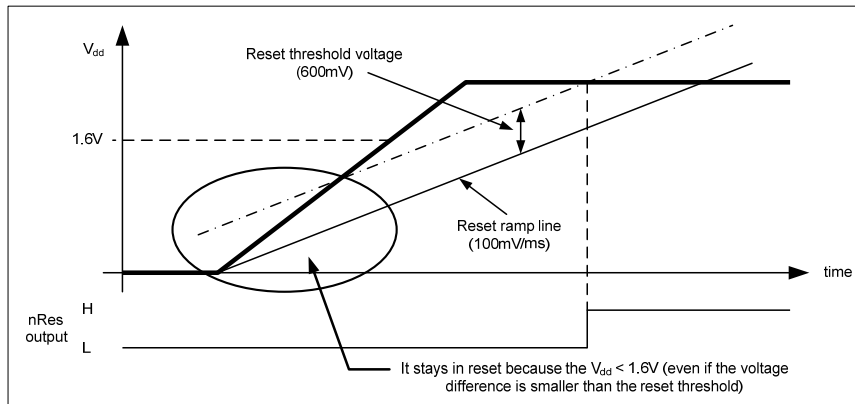
- Power-on reset: During a power up sequence until the V_{dd} has reached the correct level and stabilized
- Power glitch reset: Transients present on the V_{dd} line
- Software reset: Special control command received by the chip

Power-on reset

After power up the supply voltage starts to rise from 0V. The reset block has an internal ramping voltage reference (reset-ramp signal), which is rising at 100mV/ms (typical) rate. The chip remains in reset state while the voltage difference between the actual V_{dd} and the internal reset-ramp signal is higher than the reset threshold voltage, which is 600 mV (typical). As long as the V_{dd} voltage is less than 1.6V (typical) the chip stays in reset mode regardless the voltage difference between the V_{dd} and the internal ramp signal.

The reset event can last up to 150ms supposing that the V_{dd} reaches 90% its final value within 1ms. During this period the chip does not accept control commands via the serial control interface.

Power-on reset example:



Power glitch reset

The internal reset block has two basic mode of operation: normal and sensitive reset. The default mode is sensitive, which can be changed by the appropriate control command (see *Related control commands* at the end of this section). In normal mode the power glitch detection circuit is disabled.

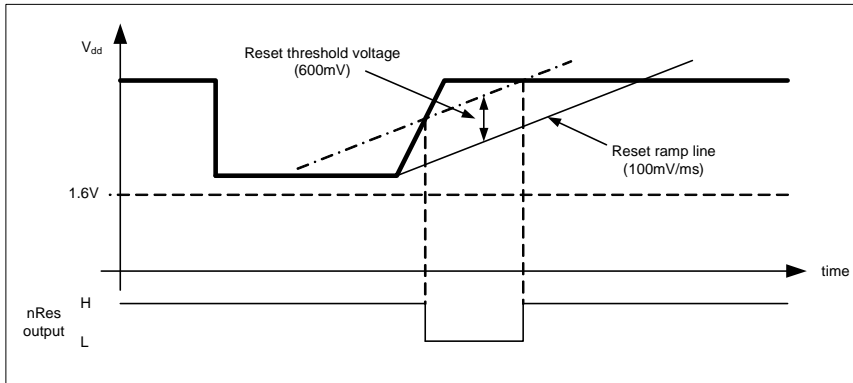
There can be spikes or glitches on the V_{dd} line if the supply filtering is not satisfactory or the internal resistance of the power supply is too high. In such cases if the sensitive reset is enabled an (unwanted) reset will be generated if the positive going edge of the V_{dd} has a rising rate greater than 100mV/ms and the voltage difference between the internal ramp signal and the V_{dd} reaches the reset threshold voltage (600 mV). Typical case when the battery is weak and due to its increased internal resistance a sudden decrease of the current consumption (for example turning off the power amplifier) might lead to an increase in supply voltage. If for some reason the sensitive reset cannot be disabled step-by-step decrease of the current consumption (by turning off the different stages one by one) can help to avoid this problem.

Any negative change in the supply voltage will not cause reset event unless the V_{dd} level reaches the reset threshold voltage (250mV in normal mode, 1.6V in sensitive reset mode).

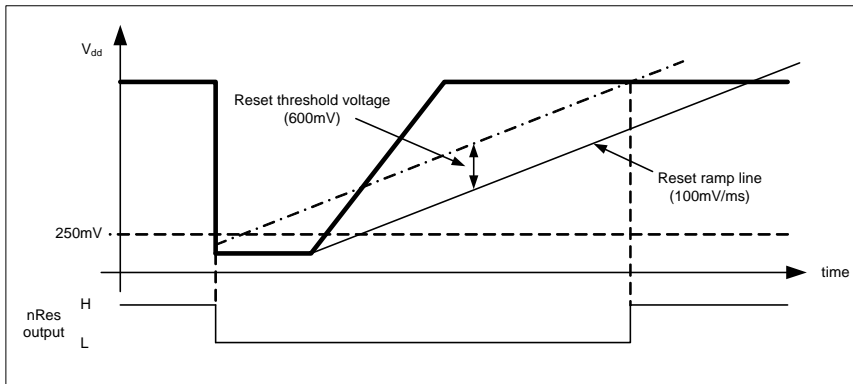
If the sensitive mode is disabled and the power supply turned off the V_{dd} must drop below 250mV in order to trigger a power-on reset event when the supply voltage is turned back on. If the decoupling capacitors keep their charges for a long time it could happen that no reset will be generated upon power-up because the power glitch detector circuit is disabled.

Note that the reset event reinitializes the internal registers, so the sensitive mode will be enabled again.

Sensitive Reset Enabled, Ripple on V_{dd} :



Sensitive reset disabled:



Software reset

Software reset can be issued by sending the appropriate control command (described at the end of the section) to the chip. The result of the command is the same as if power-on reset was occurred. When the nRES pin connected to the reset pin of the microcontroller, using the software reset command may cause unexpected problems.

V_{dd} line filtering

During the reset event (caused by power-on, fast positive spike on the supply line or software reset command) it is very important to keep the V_{dd} line as smooth as possible. Noise or periodic disturbing signal superimposed the supply voltage may prevent the part getting out from reset state. To avoid this phenomenon use adequate filtering on the power supply line to keep the level of the disturbing signal below 10mV_{p-p} in the DC – 50kHz range for 200ms from V_{dd} ramp start.. Typical example when a switch-mode regulator is used to supply the radio, switching noise may be present on the V_{dd} line. Follow the manufacturer's recommendations how to decrease the ripple of the regulator IC and/or how to shift the switching frequency.

Related control commands

"Reset Mode Command"

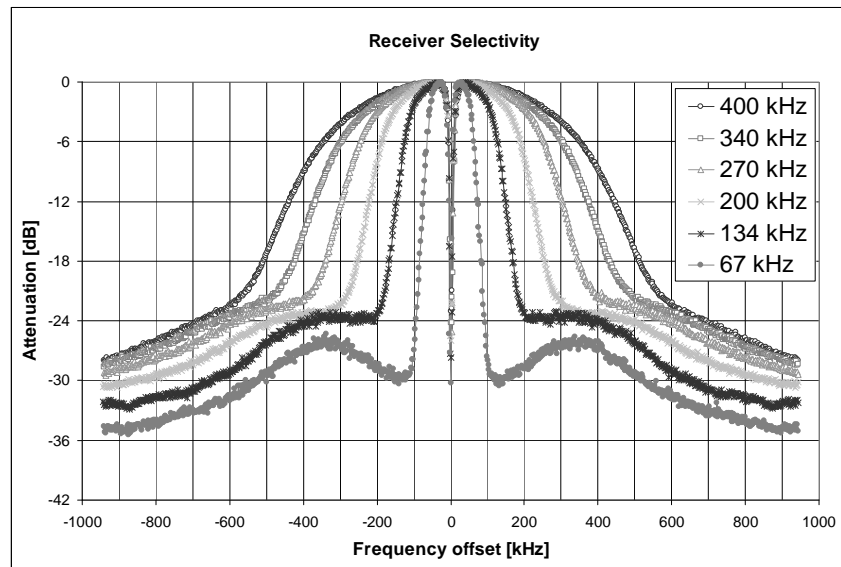
Setting bit<0> to high will change the reset mode to normal from the default sensitive.

"SW Reset Command"

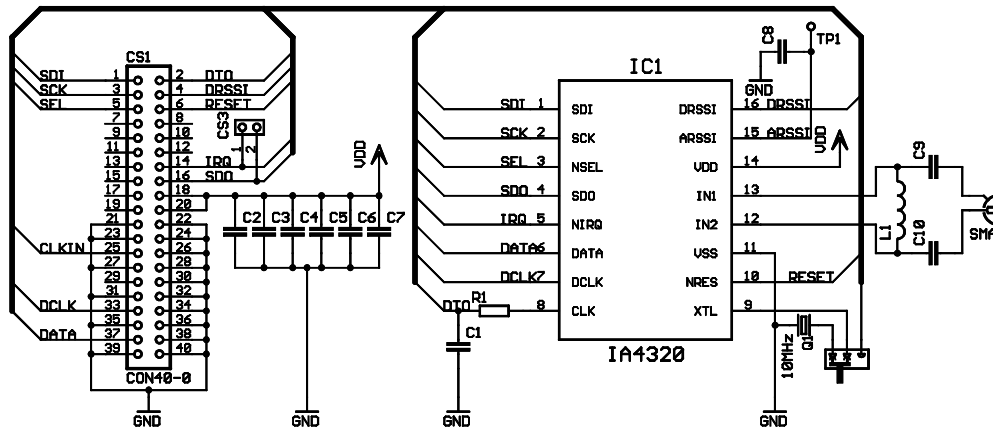
Issuing FF00h command will trigger software reset. See the *Wake-up Timer Command*.

MEASUREMENT RESULTS

Receiver Selectivity at Different Baseband Filter Settings

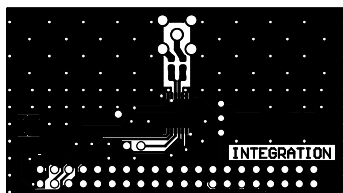


Measurement Setup

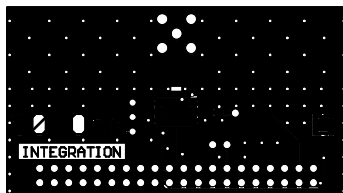


A group of decoupling capacitors is placed to provide very low supply noise for the measurements. R1-C1 forms a low pass filter to block the CLK signal going down to the test-board on pin 2 of the connector.

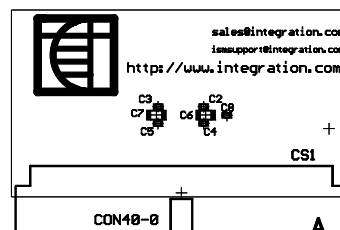
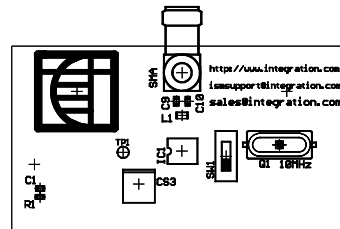
Layout and Assembly Drawing for the 50 Ω Test-Board



Top Layer

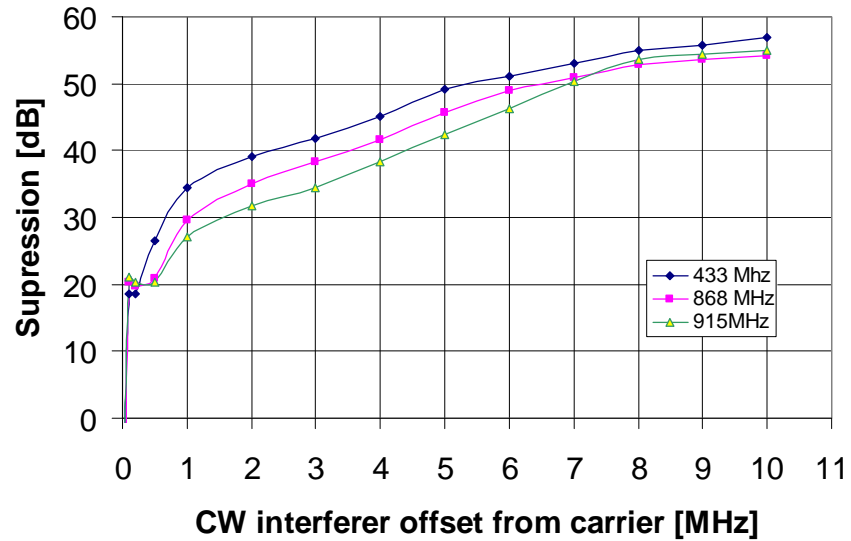


Bottom Layer



TYPICAL PERFORMANCE CHARACTERISTICS

Channel Selectivity and Blocking

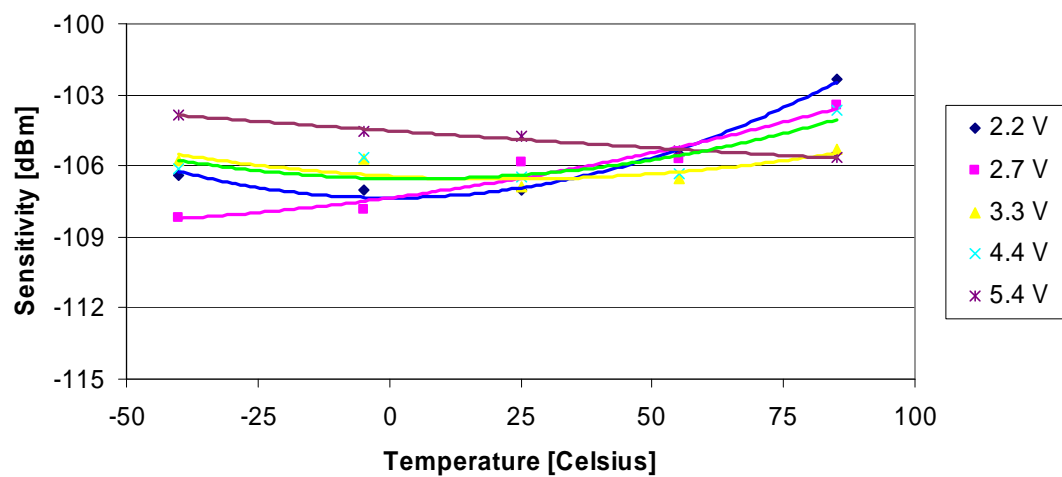


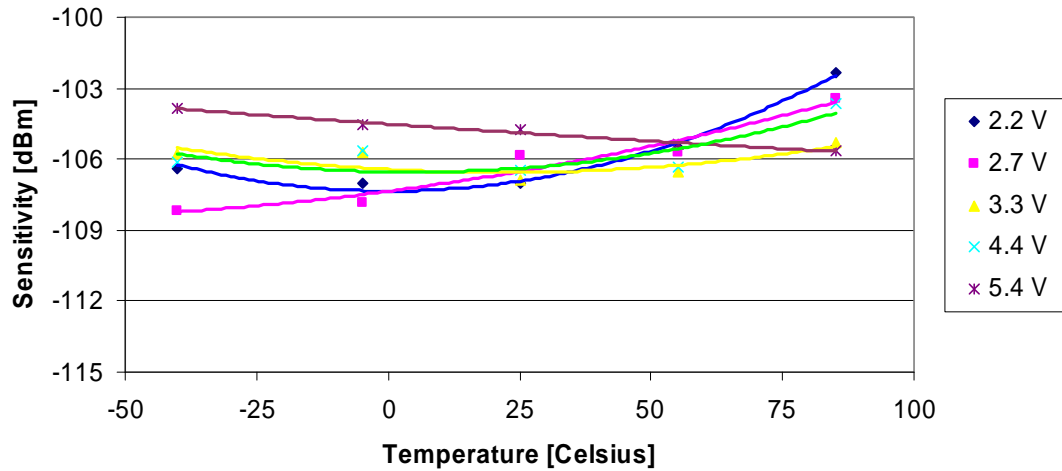
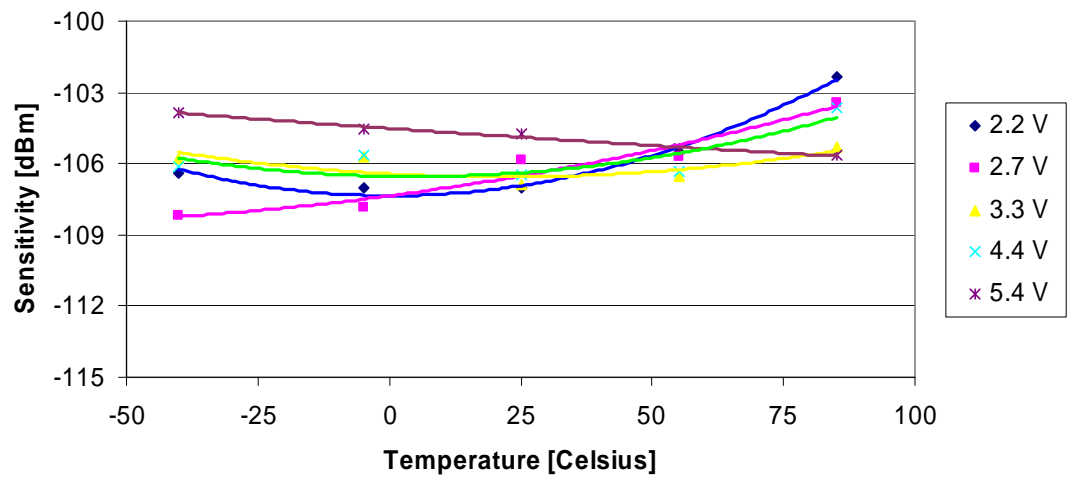
Note:

- LNA gain maximum, filter bandwidth 67 kHz, data rate 9.6 kbps, AFC switched off, FSK deviation +/- 45 kHz, V_{dd} 3V,
- Measured in compliant with ETSI Standard EN 300 220-1 v2.1.1 (2006-01 Final Draft), section 9

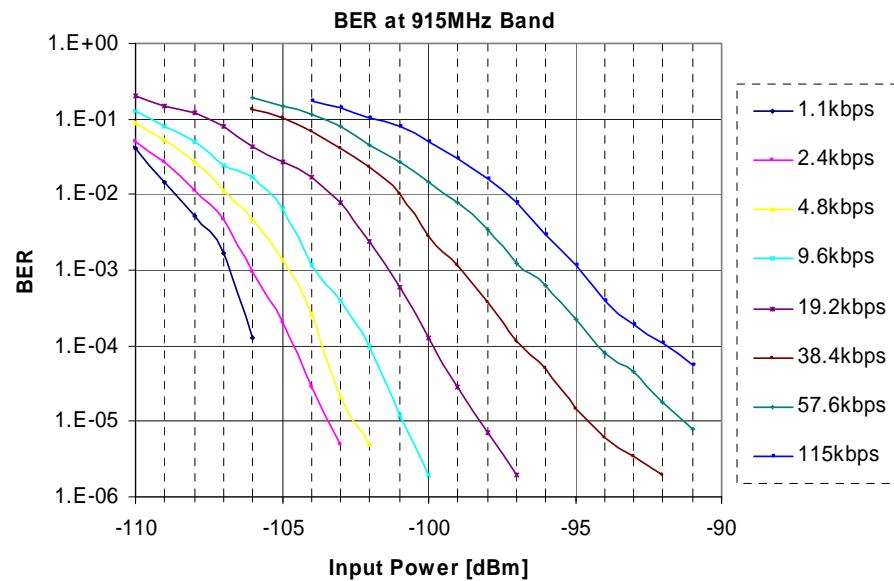
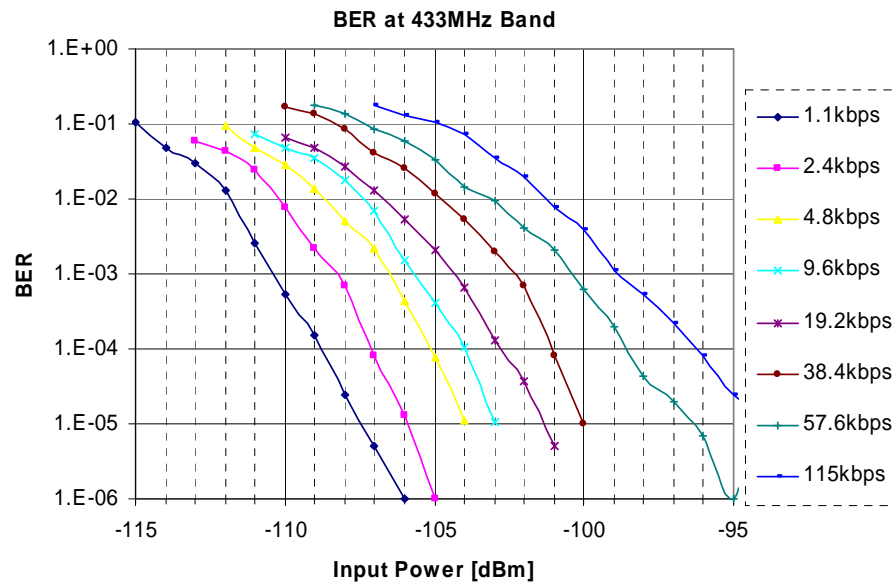
Sensitivity over Ambient Temperature (868 MHz, 9.6 kbps, dfsk: 45 kHz, BW: 67 kHz)

868 MHz



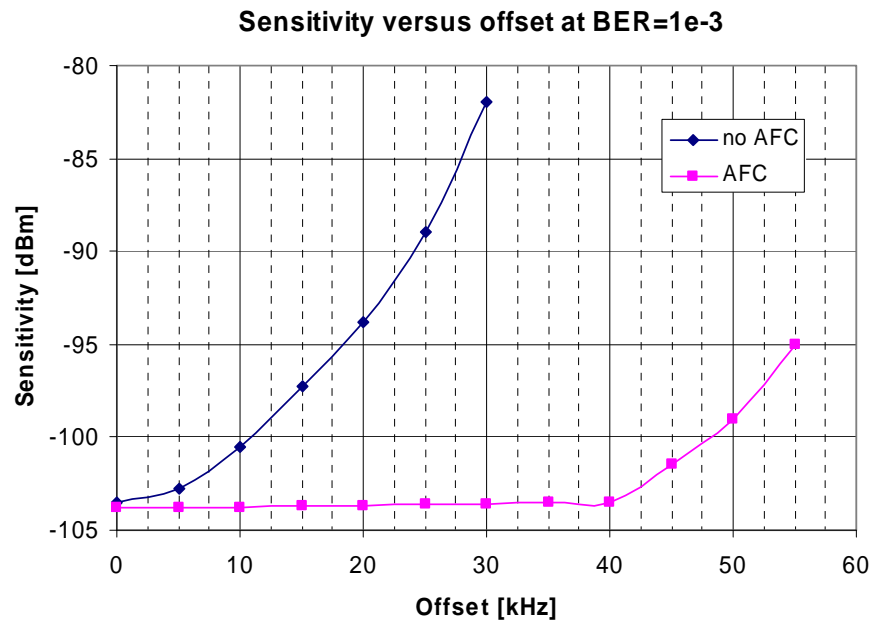
Sensitivity over Ambient Temperature (434 MHz, 9.6 kbps, dfsk: 45 kHz, BW: 67 kHz)**434 MHz****Sensitivity over Ambient Temperature (915 MHz, 9.6 kbps, dfsk: 45 kHz, BW: 67 kHz)****915 MHz**

BER Measurement Results

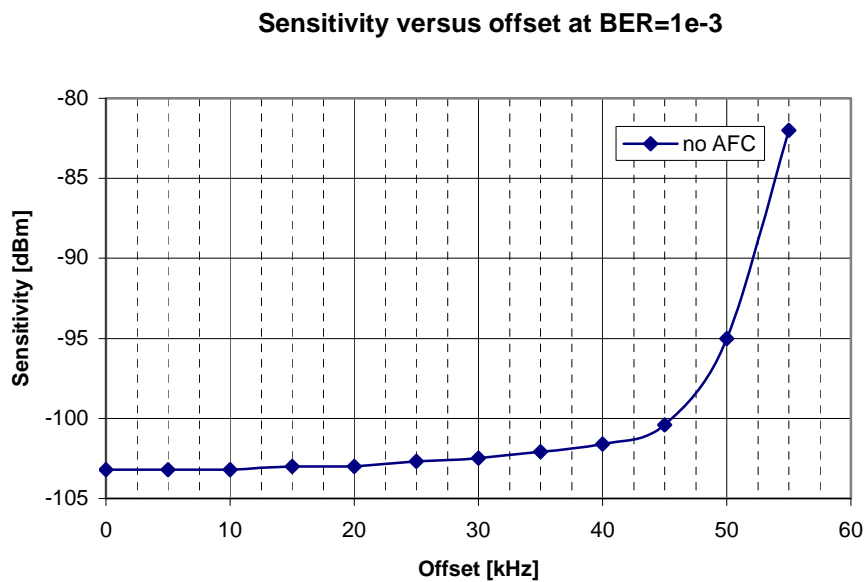


1.134 kbps	2.4 kbps	4.8 kbps	9.6 kbps	19.2 kbps	38.4 kbps	57.6 kbps	115 kbps
BW=67 kHz $\delta f_{FSK} \approx 30$ kHz	BW=67 kHz $\delta f_{FSK} \approx 30$ kHz	BW=67 kHz $\delta f_{FSK} \approx 30$ kHz	BW=67 kHz $\delta f_{FSK} \approx 45$ kHz	BW=67 kHz $\delta f_{FSK} \approx 45$ kHz	BW=134 kHz $\delta f_{FSK} \approx 90$ kHz	BW=134 kHz $\delta f_{FSK} \approx 90$ kHz	BW=200 kHz $\delta f_{FSK} \approx 120$ kHz

The table shows the optimal BW and δf_{FSK} selection for different data rates. Recommended only when using accurate crystal (20ppm or better).

Frequency Offset Effecter Sensitivity Degradation

BR=9.6 kbps, BER=10⁻³, BW=67 kHz, δf_{FSK} =60 kHz

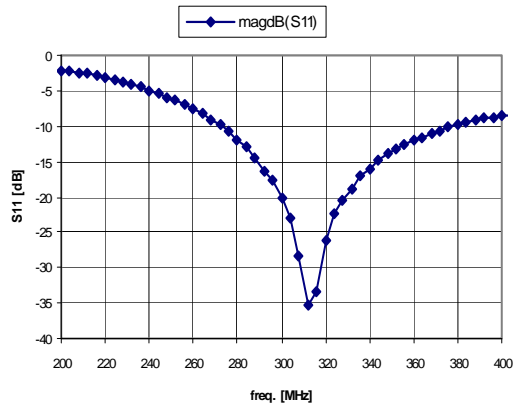


BR=9.6 kbps, BER=10⁻³, BW=134 kHz, δf_{FSK} =60 kHz

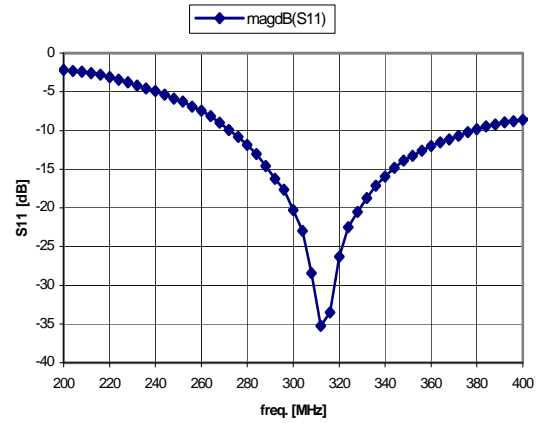
Input impedance

Measured input return loss on the demo boards with suggested matching circuit

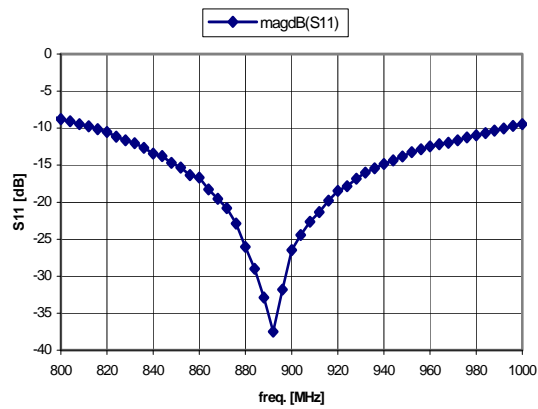
315 MHz Matching to 50 Ohm



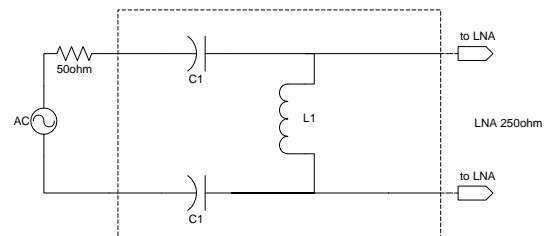
433 MHz Matching to 50 Ohm



868 and 915 MHz Matching to 50 Ohm



Input Matching circuit

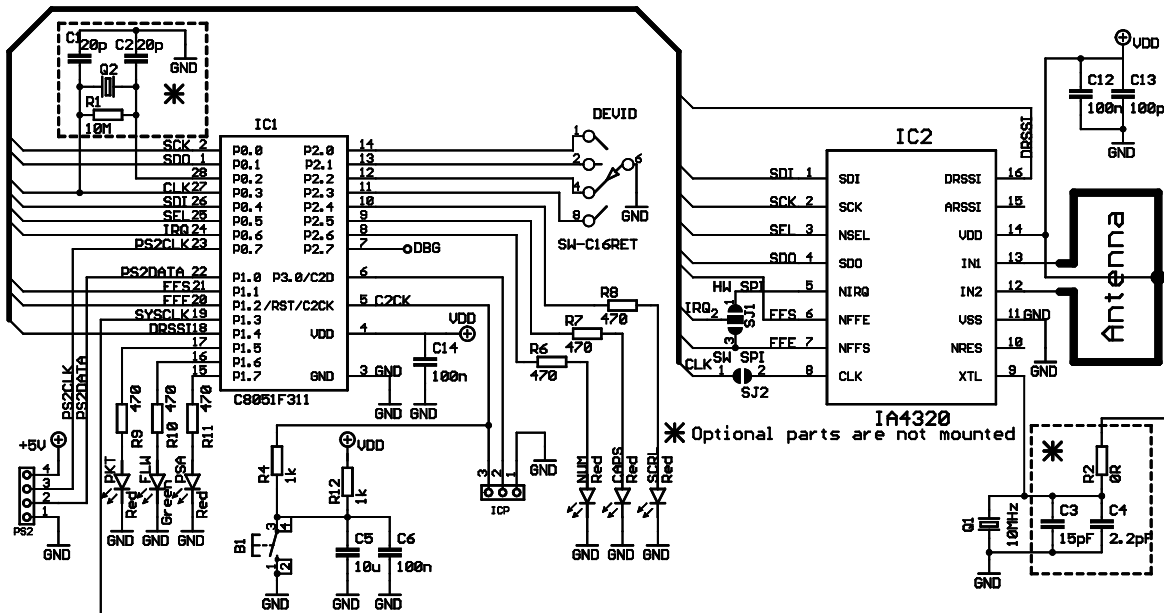


Frequency [MHz]	L1 [nH]	C1 [pF]
915	15	3
868	15	3
433	36	7
315	56	9

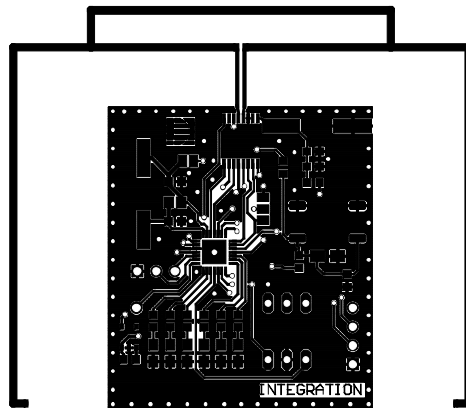
EXAMPLE APPLICATIONS

For Microcontroller Mode

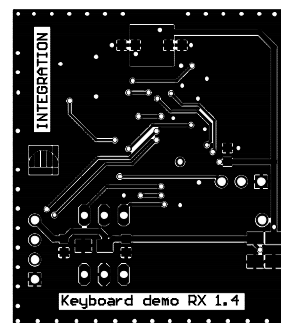
Schematic



PCB Layout of Wireless Keyboard Demo Receiver (operating in the 915 MHz band)



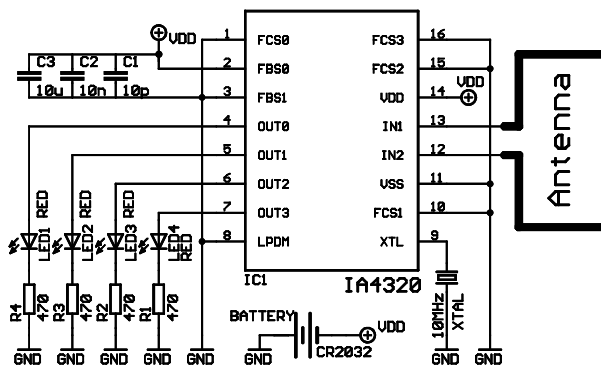
Top Layer



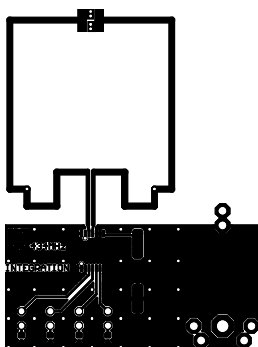
Bottom Layer

Push-Button Demo Receiver (434 MHz)

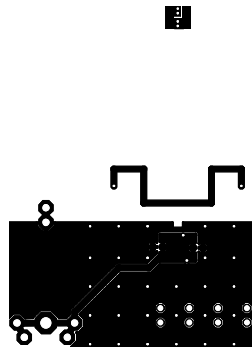
Schematics



PCB Layout of Push-Button Receiver Demo Circuit (operating in the 434 MHz band)



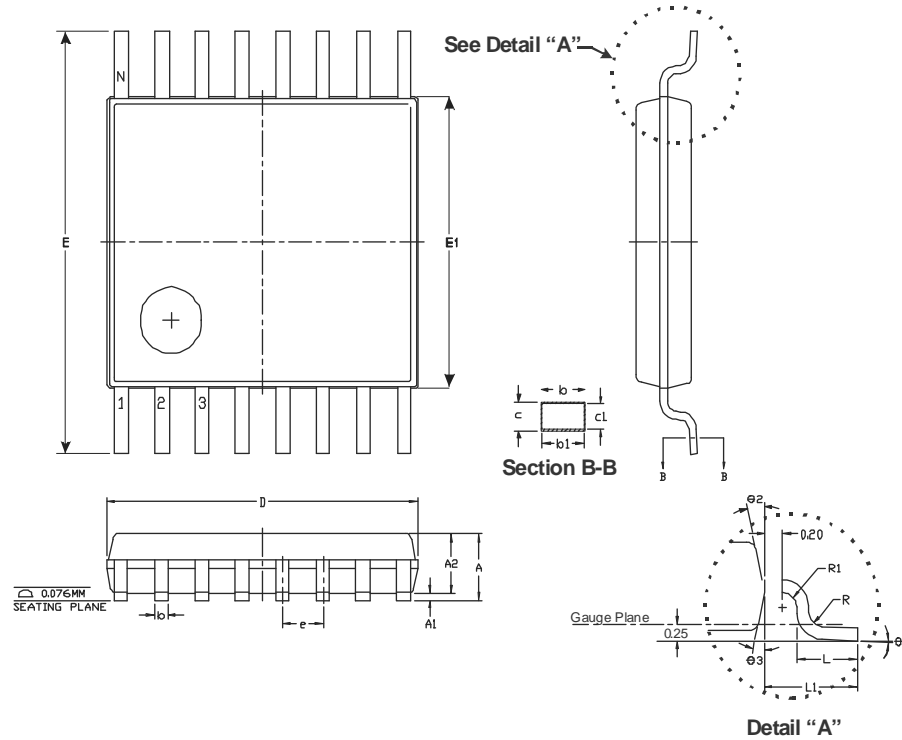
Top Layer



Bottom Layer

PACKAGE INFORMATION

16-pin TSSOP



Symbol	Dimensions in mm			Dimensions in Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A			1,20			0,047
A1	0,05		0,15	0,002		0,006
A2	0,80	0,90	1,05	0,031	0,035	0,041
b	0,19		0,30	0,007		0,012
b1	0,19	0,22	0,25	0,007	0,009	0,010
c	0,09		0,20	0,004		0,008
c1	0,09		0,16	0,004		0,006
D	4,90	5,00	5,10	0,193	0,197	0,201
e	0.65 BSC.			0.026 BSC.		
E	6.40 BSC.			0.252 BSC.		
E1	4,30	4,40	4,50	0,169	0,173	0,177
L	0,50	0,60	0,75	0,020	0,024	0,030
L1	1.00 REF.			0.39 REF.		
R	0,09			0,004		
R1	0,09			0,004		
θ1	0		8	0		8
θ2	12 REF.			12 REF.		
θ3	12 REF.			12 REF.		

RELATED PRODUCTS AND DOCUMENTS

Si4320 Universal ISM Band FSK Receiver

DESCRIPTION	ORDERING NUMBER
Si4320 16-pin TSSOP	Si4320-IC CC16 Rev J1
die	see Silicon Labs

Demo Boards and Development Kits

DESCRIPTION	ORDERING NUMBER
Development Kit	IA ISM – DK
Remote Temperature Monitoring Station	IA ISM – DATD

Related Resources

DESCRIPTION	ORDERING NUMBER
Antenna Selection Guide	IA ISM – AN1
Antenna Development Guide	IA ISM – AN2
Si4220 Universal ISM Band FSK Transmitter	See www.silabs.com/integration for details

Note: Volume orders must include chip revision to be accepted.

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wireless@silabs.com

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