Absolute Maximum Ratings (Note 1)

Input Supply Voltage ($+V_{IN}$) 40V
Sense Inputs ..... $+V_{IN}$
SCR Trigger Current (Note 2) 300mA
Indicator Output Voltage 40V
Indicator Output Sink Current 50mA
Operating Junction Temperature
  Hermetic (J, L Packages) ..... 150°C
  Plastic (N, DW Packages) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C

RoHS Peak package Solder Reflow Temp. (40 sec. max. exp.)..... 260°C (+0. -5)

Note 1. Values beyond which damage may occur.
Note 2. At higher input voltages, a dissipation limiting resistor, R_G is required. See Figure 1.

Thermal Data

J Package:
  Thermal Resistance-Junction to Case, θ_{JC} ..... 30°C/W
  Thermal Resistance-Junction to Ambient, θ_{JA} .... 80°C/W
N Package:
  Thermal Resistance-Junction to Case, θ_{JC} ..... 40°C/W
  Thermal Resistance-Junction to Ambient, θ_{JA} ..... 65°C/W
DW Package:
  Thermal Resistance-Junction to Case, θ_{JC} ..... 40°C/W
  Thermal Resistance-Junction to Ambient, θ_{JA} ..... 95°C/W
L Package:
  Thermal Resistance-Junction to Case, ... 35°C/W
  Thermal Resistance-Junction to Ambient, θ_{JA} ..... 120°C/W

Note A. Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.

Note B. The above numbers for θ_{JC} are maximums for the limiting thermal resistance of the package in a standard mounting configuration. The θ_{JA} numbers are meant to be guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

Recommended Operating Conditions (Note 3)

Input Supply Voltage ($+V_{IN}$) ..... 4.7V to 40V
Current Limit Common Mode
Input Voltage Range ..... 0V to $+V_{IN}$ -3V
Reference Load Current ..... 0 to 10mA
Indicator Output Voltage ..... 4.7V to 40V
Indicator Output Current ..... 0 to 10mA
Delay Timing Capcitor (Note 4) ..... 0 to 1µF
Operating Ambient Temperature Range
SG1543 ..... -55°C to 125°C
SG2543 ..... -25°C to 85°C
SG3543 ..... 0°C to 70°C

Note 3: Range over which the device is functional.
Note 4. Larger value capacitor may be used with peak current limiting. See Figure 7.

Electrical Characteristics

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG1543 with -55°C ≤ T_A ≤ 125°C, SG2543 with -25°C ≤ T_A ≤ 85°C, SG3543 with 0°C ≤ T_A ≤ 70°C, and $+V_{IN}$ = 10V. Indicator outputs have 2kΩ pull-up resistor. Low duty cycle testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG1543/SG2543			SG3543			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply Section								
Input Voltage Range	T_J = 25°C to T_{MAX}	4.5		40	4.5		40	V
		4.7		40	4.7		40	V
Supply Current	$+V_{IN}$ = 40V, Outputs open, T_J = 25°C		7	10		7	10	mA
Reference Section								
Output Voltage	T_J = 25°C	2.48	2.50	2.52	2.45	2.50	2.55	V
		2.45		2.55	2.40		2.60	V
Line Regulation	$+V_{IN}$ = 5 to 30V		1	5		1	5	mV
Load Regulation	I_{REF} = 0 to 10mA		1	10		1	10	mV
Short Circuit Current	V_{REF} = 0V	12	25	40	12	25	40	mA
Temperature Stability			.005			.005		%/°C

Electrical Characteristics (Continued)

Parameter	Test Conditions	SG1543/SG2543			SG3543			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Comparator Section								
Input Threshold (Note 5)	T_J = 25°C	2.45	2.50	2.55	2.40	2.50	2.60	V
		2.40		2.60	2.35		2.65	V
Input Hysteresis			25			25		mV
Input Bias Current	Sense input = 0V		0.3	1.0		0.3	1.0	µA
Delay Saturation			0.2	0.5		0.2	0.5	V
Delay High Level			6	8		6	8	V
Delay Charging Current	V_D = 0V	200	250	300	200	250	300	µA
Indicate Saturation	I_L = 10mA		0.2	0.5		0.2	0.5	V
Indicate Leakage	V_{IND} = 40V		.01	1.0		0.1	1.0	µA
Propagation Delay	$V_{O.V.\ INPUT}$ = 2.7V, $V_{U.V.\ INPUT}$ = 2.3V, T_J = 25°C							
	C_D = 0		400			400		ns
	C_D = 1µF		10			10		ms
SCR Trigger Section								
Peak Output Current	$+V_{IN}$ = 5V, R_G = 0, V_O = 0	100	200	400	100	200	400	mA
Peak Output Voltage	$+V_{IN}$ = 15V, I_O = 100mA	12	13		12	13		V
Output Off Voltage	$+V_{IN}$ = 40V, R_L = 1kΩ		0	0.1		0	0.1	V
Remote Activate Current	REM. ACT. pin = Gnd		0.4	0.8		0.4	0.8	mA
Remote Activate Voltage	REM. ACT pin open		2	6		2	6	V
Reset Current	RESET pin = Gnd, REM. ACT. = Gnd		0.4	0.8		0.4	0.8	mA
Reset Voltage	RESET pin open, REM. ACT. = Gnd		2	6		2	6	V
Output Current Rise Time	R_L = 50Ω, T_J = 25°C, C_D = 0		400			400		mA/µs
Prop. Delay from REM. ACT. Pin	$V_{REM.\ ACT.}$ = 0.4V		300			300		ns
Prop. Delay fom O.V. INPUT Pin	$V_{O.V.\ INPUT}$ = 2.7V		500			500		ns
Current Limit Section								
Input Voltage Range		0		V_{IN}-3V	0		V_{IN}-3V	V
Input Bias Current	OFFSET/COMP pin open, V_{CM} = 0V		0.3	1.0		0.3	1.0	µA
Input Offset Voltage	OFFSET/COMP pin open, V_{CM} = 0V,		0	10		0	15	mV
	10kΩ from OFFSET/COMP pin to Gnd, T_J =25°C	80	100	120	70	100	130	mV
CMRR	$0 \le V_{CM} \le 12V$, V_{IN} = 15V	60	70		60	70		dB
AVOL	OFFSET/COMP pin open, V_{CM} = 0V	72	80		72	80		dB
Output Saturation	I_L = 10mA		0.2	0.5		0.2	0.5	V
Output Leakage	V_{IND} = 40V		.01	1.0		.01	1.0	µA
Small Signal Bandwidth	A_V = 0dB, T_J = 25°C		5			5		MHz
Propagation Delay	$V_{OVERDRIVE}$ = 100mV, T_J = 25°C		200			200		ns

Note 5. Input voltage rising on O.V. Input and falling on U.V. Input.

Characteristics Curves

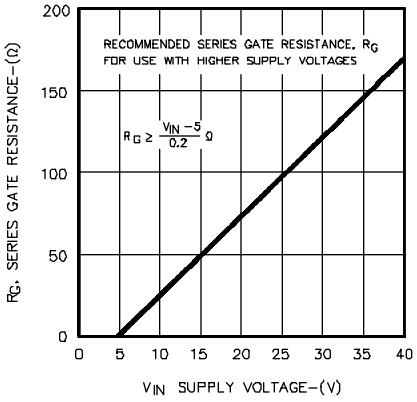


Figure 1 · SCR Trigger Power Limiting

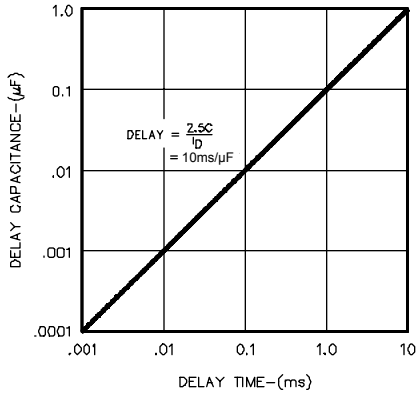


Figure 2 · Activation Delay Vs. Capacitor Value

Characteristics Curves (Continued)

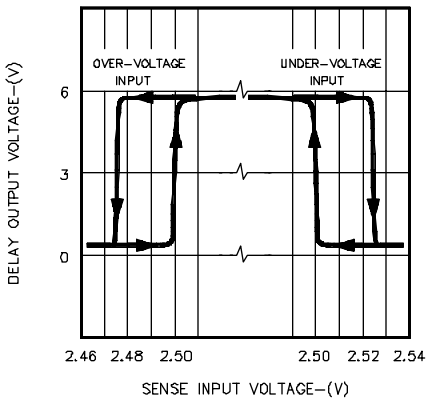


Figure 3 · Comparator Input Hysteresis

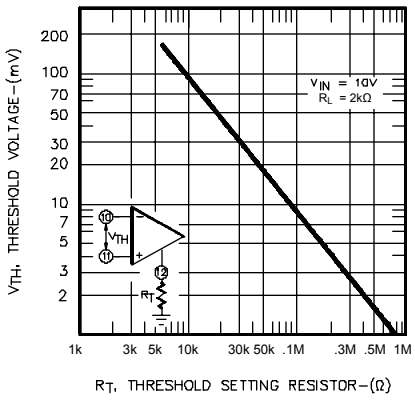


Figure 4 · Current Limit Input Threshold

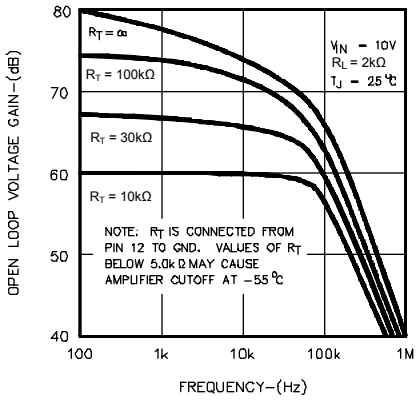


Figure 5 · Current Limit Amplifier Gain

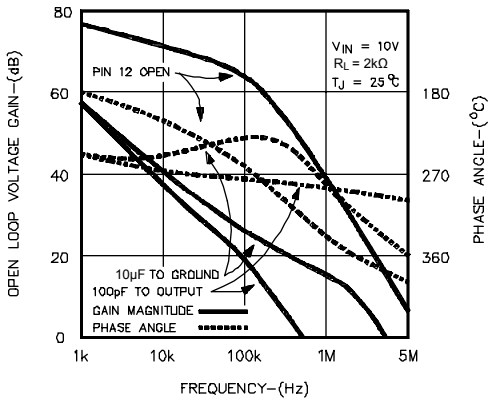


Figure 6 · Current Limit Amplifier Frequency Response

Application Information

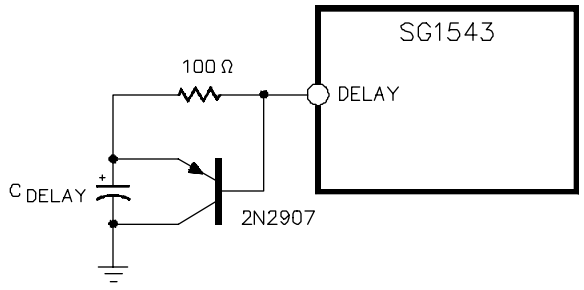


Figure 7 · Surge Limit Circuit for Large Delay Capacitors

The 100 ohm resistor limits the peak discharge current into the SG1543 while the external PNP transistor provides a high peak-current discharge path for the delay capacitor.

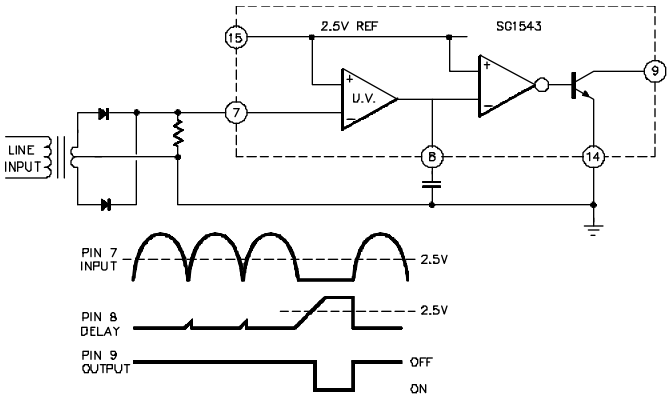


Figure 8 · Input Line Monitor

Application Information (Continued)

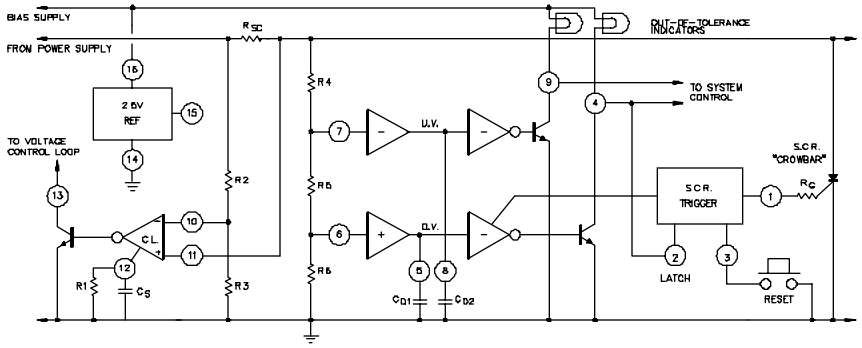


Figure 9 · Typical Application Circuit

The values for the external components are determined as follows:

Current limit input threshold, $V_{TH} \approx \frac{1000}{R_1}$

C_S is determined by the current loop dynamics

Peak current to load, $I_P \approx \frac{V_{TH}}{R_{SC}} + \frac{V_O}{R_{SC}}\left(\frac{R_2}{R_2+R_3}\right)$

Short circuit current, $I_{SC} = \frac{V_{TH}}{R_{SC}}$

Low output voltage limit, V_O (Low) = $\frac{2.5\,(R_4+R_5+R_6)}{R_5+R_6}$

High output voltage limit, V_O (High) = $\frac{2.5\,(R_4+R_5+R_6)}{R_6}$

Voltage sensing delay, $t_D = 10{,}000\ C_D$

SCR trigger power limiting resistor, $R_G > \frac{V_{IN} - 5}{0.2}$

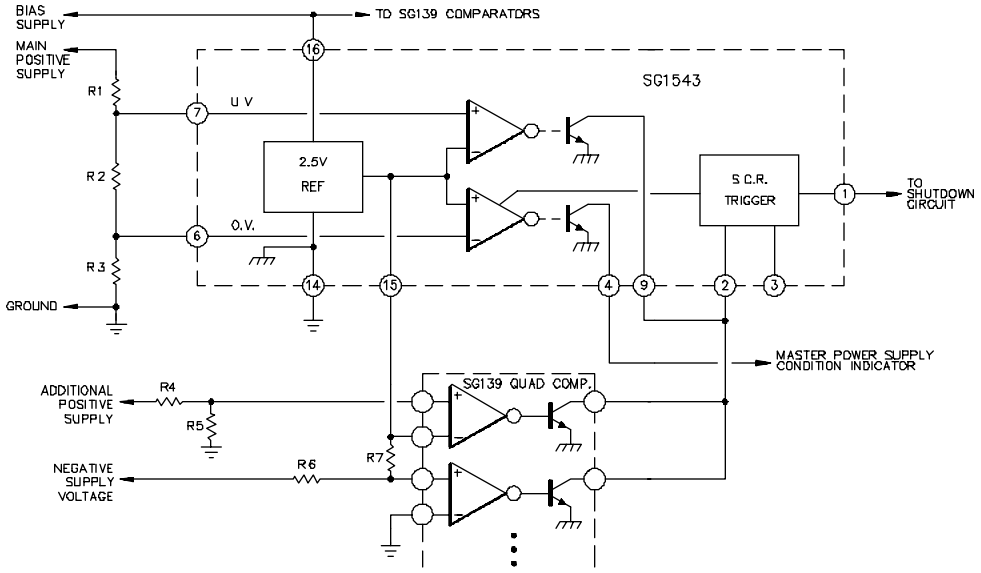


Figure 10 · Sensing Multiple Supply Voltages

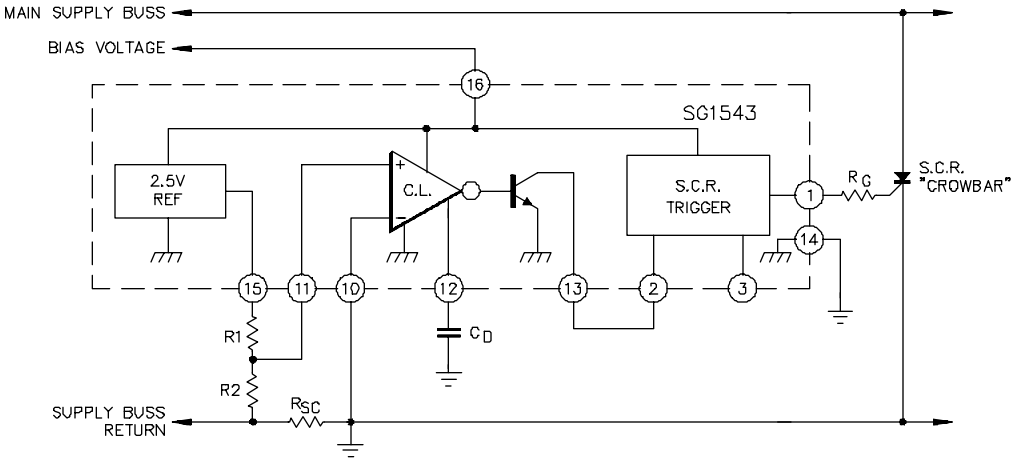
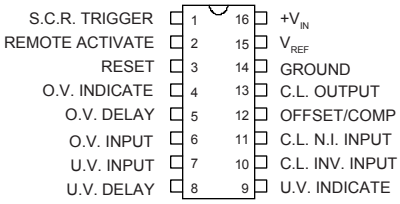
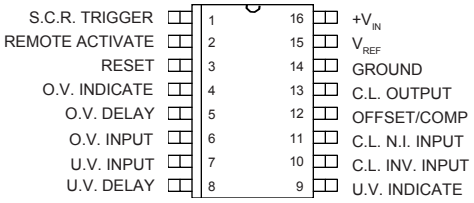
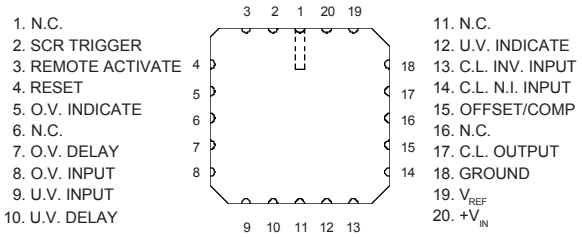


Figure 11 · Over Current Shutdown

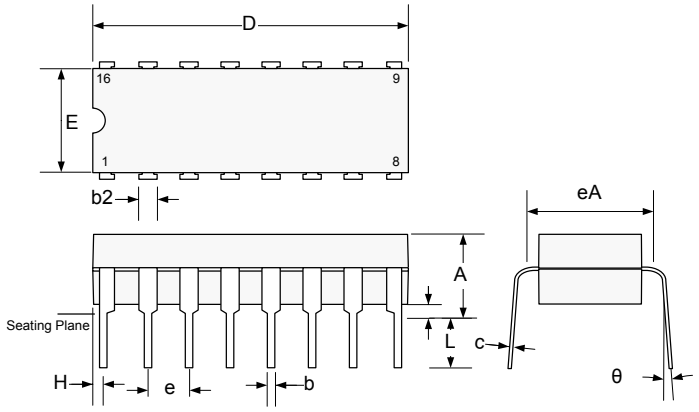
Connection Diagrams and Ordering Information (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
16-PIN CERAMIC DIP J - PACKAGE	SG1543J-883B SG1543J-DESC SG1543J	-55°C to 125°C -55°C to 125°C -55°C to 125°C	 N Package: RoHS Compliant / Pb-free Transition DC: 0503 N Package: RoHS / Pb-free 100% Matte Tin Lead Finish
16-PIN PLASTIC DIP N - PACKAGE	SG2543N SG3543N	-25°C to 85°C 0°C to 70°C	
16-PIN WIDE BODY PLASTIC SOIC DW - PACKAGE	SG2543DW SG3543DW	-25°C to 85°C 0°C to 70°C	 DW Package: RoHS Compliant / Pb-free Transition DC: 0516 DW Package: RoHS / Pb-free 100% Matte Tin Lead Finish
20-PIN CERAMIC LEADLESS CHIP CARRIER L - PACKAGE (Note 3)	SG1543L-883B SG1543L-DESC SG1543L	-55°C to 125°C -55°C to 125°C	

Note 1. Contact factory for DESC product availablity.
2. All packages are viewed from the top.
3. Consult factory for product availability.
4. Hermetic Packages J & L use Pb37/Sn63 hot solder lead finish, contact factory for availability of RoHS versions.

Package Outline Dimensions

Controlling dimensions are in inches, metric equivalents are shown for general information.

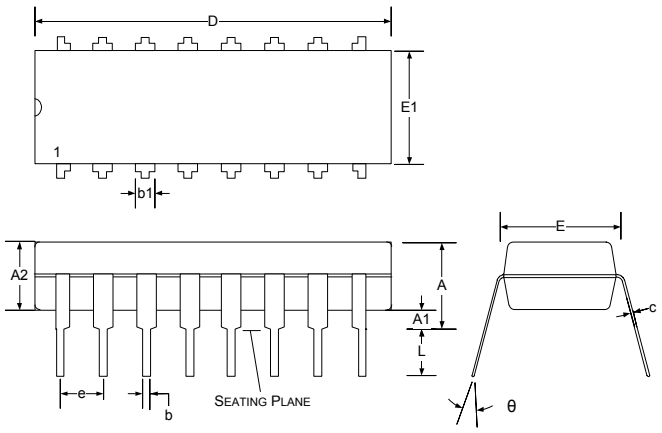


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	5.08	-	0.200
b	0.38	0.51	0.015	0.020
b2	1.04	1.65	0.045	0.065
c	0.20	0.38	0.008	0.015
D	19.30	19.94	0.760	0.785
E	5.59	7.11	0.220	0.280
e	2.54 BSC		0.100 BSC	
eA	7.37	7.87	0.290	0.310
H	0.63	1.78	0.025	0.070
L	3.18	5.08	0.125	0.200
θ	-	15°	-	15°
Q	0.51	1.02	0.020	0.040

Note:

Dimensions do not include protrusions; these shall not exceed 0.155mm (.006”) on any side. Lead dimension shall not include solder coverage.

Figure 12 · J 16-Pin Ceramic Dip



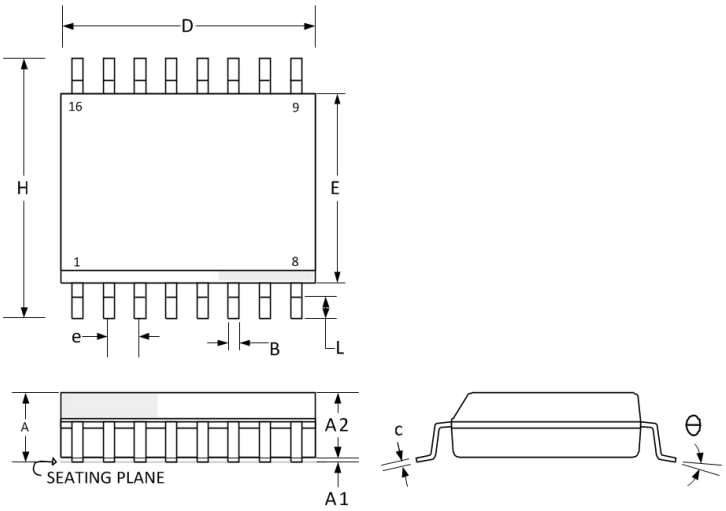
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	5.33	-	0.210
A1	0.38	-	0.015	-
A2	3.30 Typ.		0.130 Typ.	
b	0.36	0.56	0.014	0.022
b1	1.14	1.78	0.045	0.070
c	0.20	0.36	0.008	0.014
D	18.67	19.69	0.735	0.775
e	2.54 BSC		0.100 BSC	
E	7.62	8.26	0.300	0.325
E1	6.10	7.11	0.240	0.280
L	2.92	0.381	0.115	0.150
θ	-	15°	-	15°

Note:

Dimensions do not include protrusions; these shall not exceed 0.155mm (.006”) on any side. Lead dimension shall not include solder coverage.

Figure 13 · N 16-Pin Plastic Dual Inline Package Dimensions

Package Outline Dimensions (Continued)



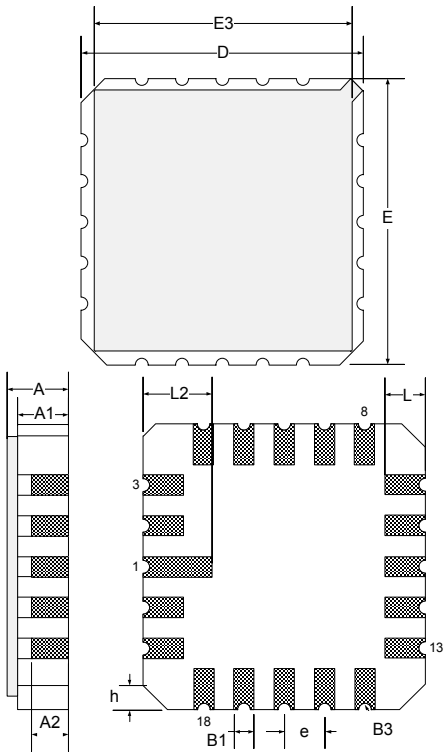
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.06	2.65	0.081	0.104
A1	0.10	0.30	0.004	0.012
A2	2.03	2.55	0.080	0.100
B	0.33	0.51	0.013	0.020
c	0.23	0.32	0.009	0.013
D	10.08	10.50	0.397	0.413
E	7.40	7.60	0.291	0.299
e	1.27 BSC		0.05 BSC	
H	10.00	10.65	0.394	0.419
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°
*LC	-	0.10	-	0.004

*Lead co planarity

Note:

Dimensions do not include protrusions; these shall not exceed 0.155mm (.006”) on any side. Lead dimension shall not include solder coverage.

Figure 14 · DW 16-Pin SOWB Package Dimensions



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
D/E	8.64	9.14	0.340	0.360
E3	-	8.128	-	0.320
e	1.270 BSC		0.050 BSC	
B1	0.635 TYP		0.025 TYP	
L	1.02	1.52	0.040	0.060
A	1.626	2.286	0.064	0.090
h	1.016 TYP		0.040 TYP	
A1	1.372	1.68	0.054	0.066
A2	-	1.168	-	0.046
L2	1.91	2.41	0.075	0.95
B3	0.203R		0.008R	

Note:

All exposed metalized area shall be gold plated 60 micro-inch minimum thickness over nickel plated unless otherwise specified in purchase order.

Figure 15 · L 20-Pin Ceramic LCC Package Outline Dimensions

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