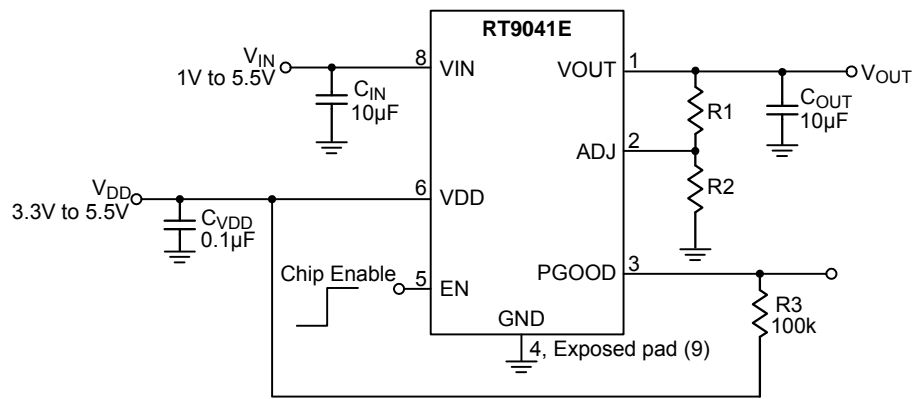


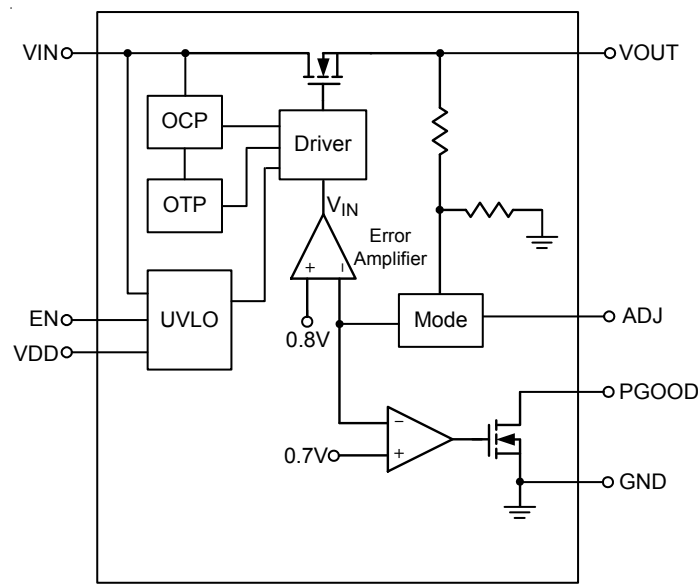
Typical Application Circuit



Function Pin Description

Pin No.	Pin Name	Pin Function
1	VOUT	Output Voltage.
2	ADJ	Output Voltage Adjust Pin. Set the output voltage by the internal feedback resistors when ADJ is ground. If external feedback resistors is used, $V_{OUT} = V_{REF} \times (R1 + R2)/R2$ .
3	PGOOD	Power Good Open Drain Output.
4, 9 (Exposed pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
5	EN	Chip Enable (Active-High).
6	VDD	Supply Voltage of Control Circuitry.
7	NC	No Internal Connection.
8	VIN	Supply Input Voltage.

Function Block Diagram



## Absolute Maximum Ratings (Note 1)

Bias Supply Input Voltage, VDD	6V
Supply Input Voltage, VIN	6V
Other Input/Output Pins	6V
Power Dissipation, PD @ TA = 25°C	
WDFN-8L 2x2	0.833VW
Package Thermal Resistance (Note 2)	
WDFN-8L 2x2, $\theta_{JA}$	120°C/W
WDFN-8L 2x2, $\theta_{JC}$	8.2°C/W
Lead Temperature (Soldering, 10 sec.)	260°C
Junction Temperature	150°C
Storage Temperature Range	–65°C to 150°C
ESD Susceptibility (Note 3)	
HBM (Human Body Model)	2kV

## Recommended Operating Conditions (Note 4)

Bias Supply Input Voltage, VDD	3V to 5.5V
Supply Input Voltage, VIN	1V to 5.5V
Junction Temperature Range	–40°C to 125°C
Ambient Temperature Range	–40°C to 85°C

## Electrical Characteristics

(VIN = 1.8V, ILOAD = 1mA, COUT = 10μF, TA = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>Input</b>						
Adjustable Output Voltage Range	VOUT		0.8	--	2.5	V
Bias Input Under Voltage Lockout	VUVLO		--	2.7	--	V
VIN Shutdown Current	ISHDN	1V < VIN < 5.5V, VIN = VOUT + 0.6V	--	1	5	μA
Quiescent Current	IQ	3V < VDD < 5.5V	--	160	250	μA
VDD Shutdown Current	ISHDN	3V < VDD < 5.5V	--	1	5	μA
<b>Regulator Characteristics</b>						
Line Regulation	$\Delta V_{OUT} / \Delta V_{IN}$	IOUT = 10mA, 1.5V < VIN < 5.5V, VIN = VOUT + 0.6V	–0.15	--	0.15	%/V
Load Regulation	$\Delta V_{OUT} / \Delta I_{IN}$	VIN = VOUT + 0.6V, ILOAD = 1mA to 300mA	--	0.2	1	%
Fixed Output Voltage Accuracy	$\Delta V_{OUT}$	Short ADJ to GND, IOUT = 10mA	–2	--	2	%
Reference Voltage	VREF	IOUT = 10mA	0.784	0.8	0.816	V
Dropout Voltage	VDROP	IOUT = 300mA, VDD – VOUT ≥ 2.1V	--	200	300	mV
		IOUT = 500mA, VDD – VOUT ≥ 2.1V	--	300	500	
Current Limit	ILIM	RLOAD = 0	550	700	1400	mA
Thermal-Shutdown	TSD	3V < VDD < 5.5V	--	160	--	°C
Thermal-Shutdown Hysteresis	$\Delta T_{SD}$		--	20	--	°C

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
<b>ADJ</b>							
ADJ Pin Threshold				--	0.2	--	V
<b>PGOOD Comparator</b>							
Comparator Threshold			% of regulated output voltage	--	88	--	%
Comparator Hysteresis		V <sub>HYST</sub>	(Note 5)	--	10	--	mV
<b>Logic and I/O</b>							
EN Input Voltage	Logic-High	V <sub>IH</sub>		1.6	--	--	V
	Logic-Low	V <sub>IL</sub>		--	--	0.8	
EN Current		I <sub>EN</sub>	V <sub>EN</sub> = 5V	--	12	--	μA
PGOOD Output Low Voltage			PGOOD sinking 1mA	--	--	0.1	V
PGOOD Output High Leakage Current			0 < V <sub>PGOOD</sub> < V <sub>IN</sub>	-1	--	1	μA
<b>Dynamics</b>							
PGOOD Propagation Delay		t <sub>PGOOD</sub>	Rising edge within 5% of regulation level	1	--	5	ms

**Note 1.** Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

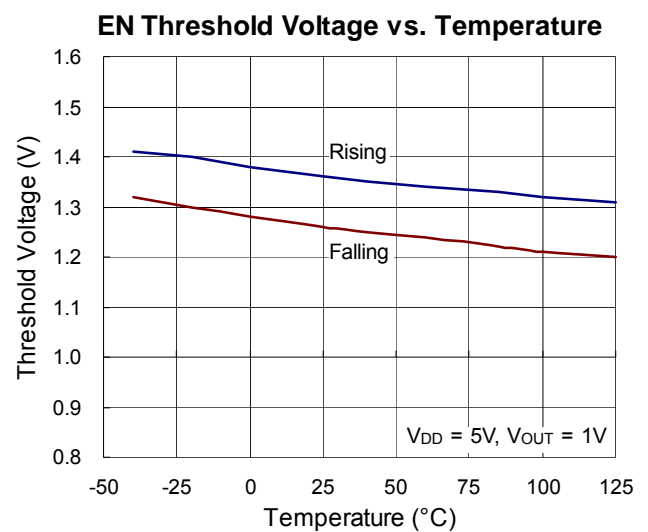
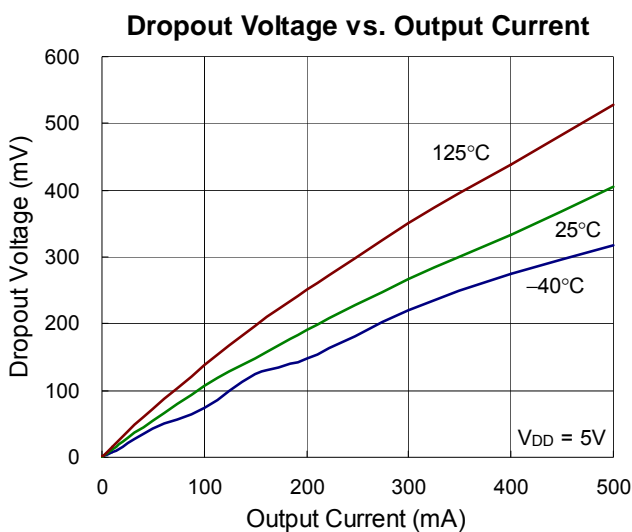
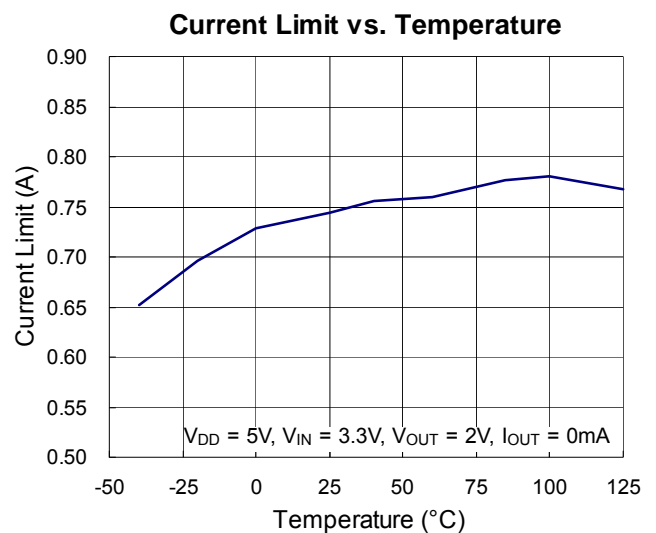
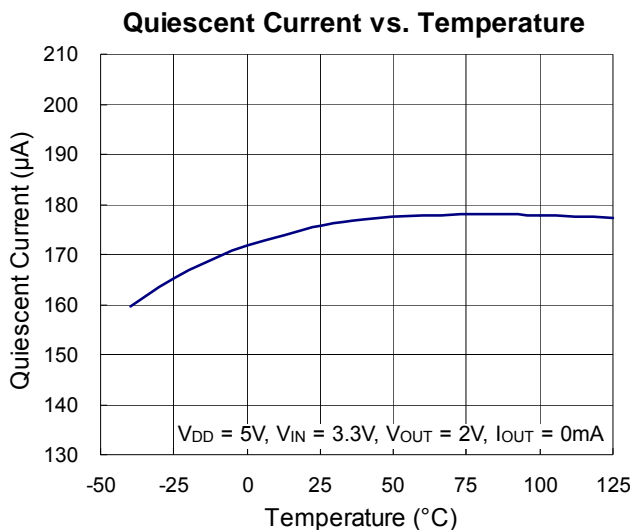
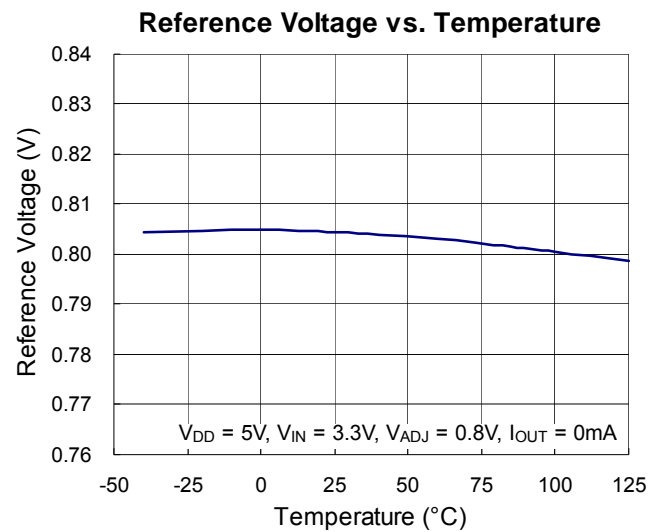
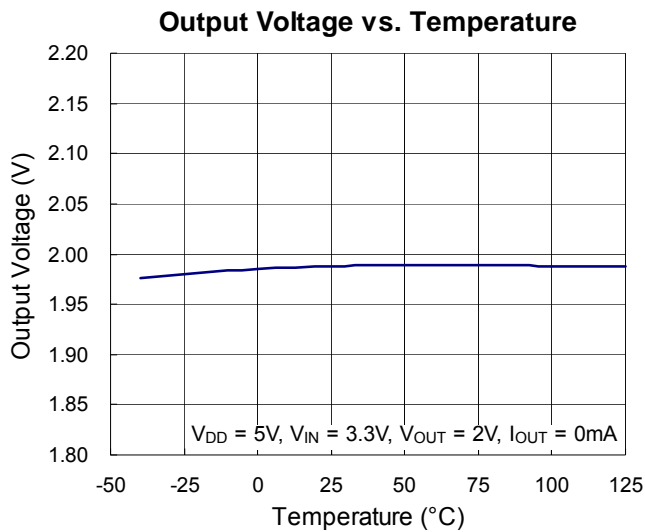
**Note 2.**  $\theta_{JA}$  is measured at  $T_A = 25^\circ\text{C}$  on a high effective thermal conductivity four-layer test board per JEDEC 51-7.  $\theta_{JC}$  is measured at the exposed pad of the package.

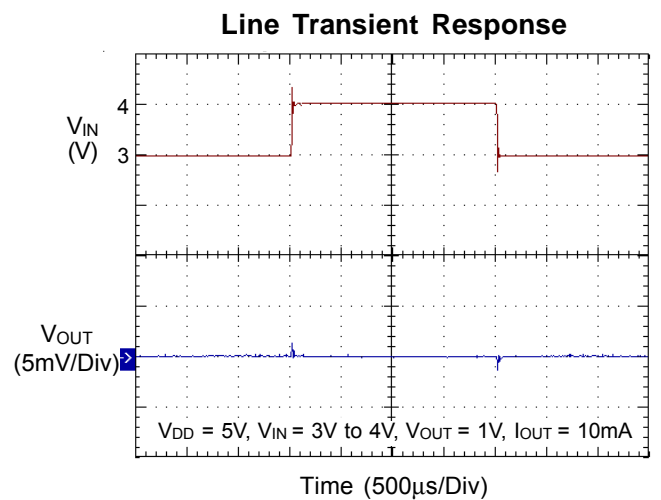
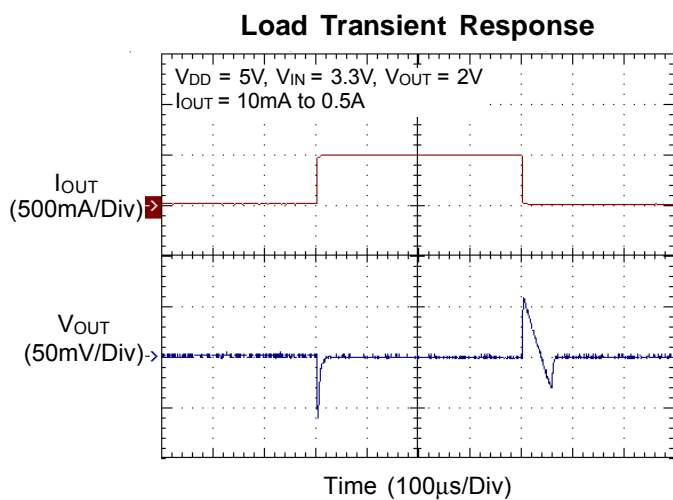
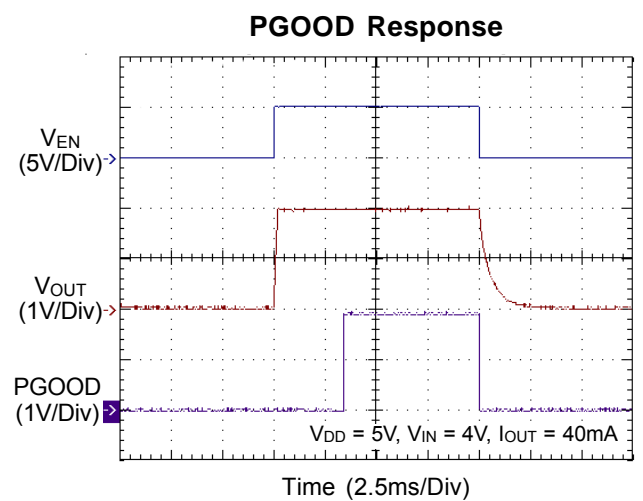
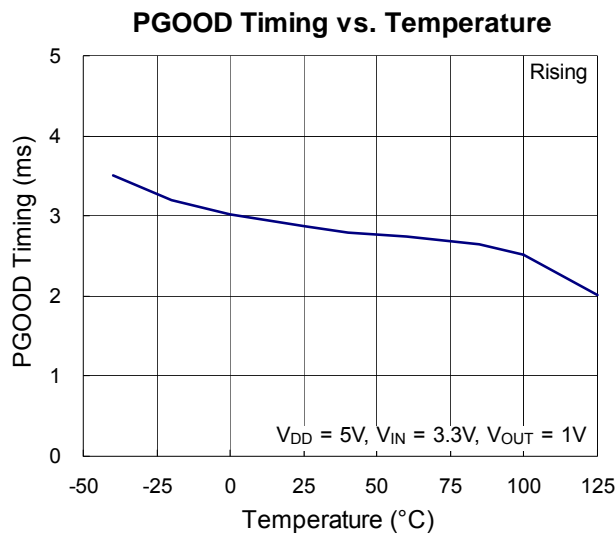
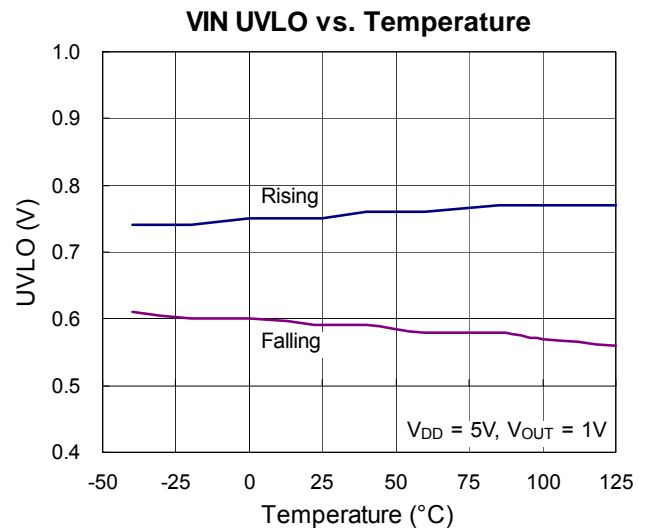
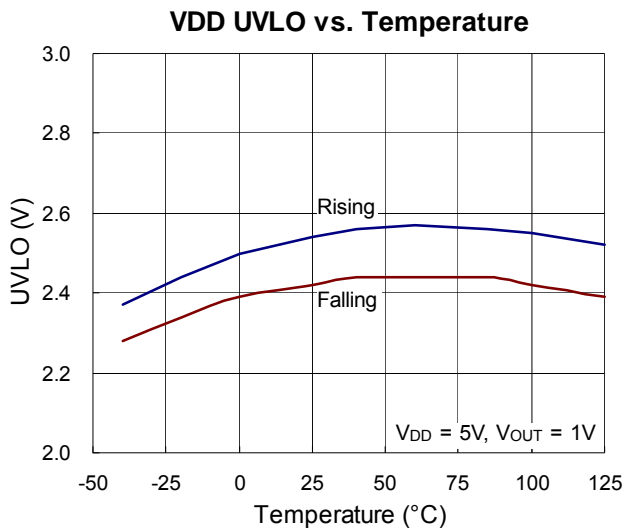
**Note 3.** Devices are ESD sensitive. Handling precaution is recommended.

**Note 4.** The device is not guaranteed to function outside its operating conditions.

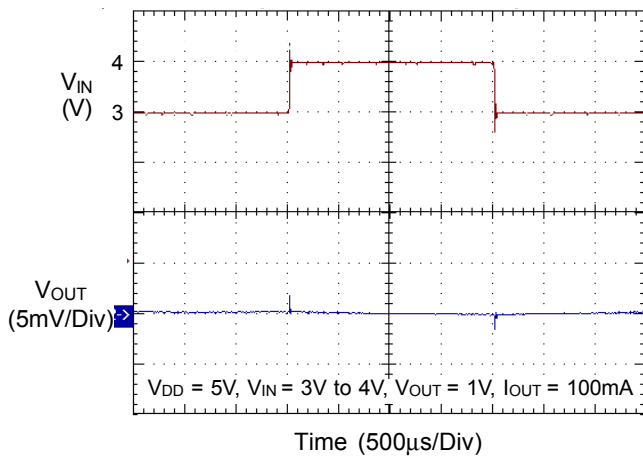
**Note 5.** Guaranteed by Design.

## Typical Operating Characteristics

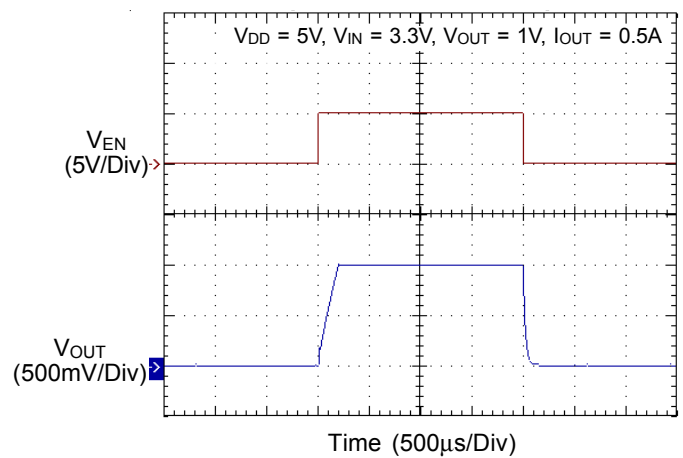




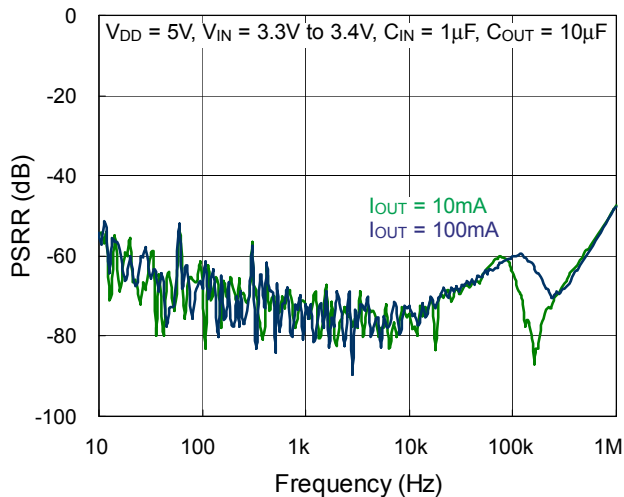
Line Transient Response



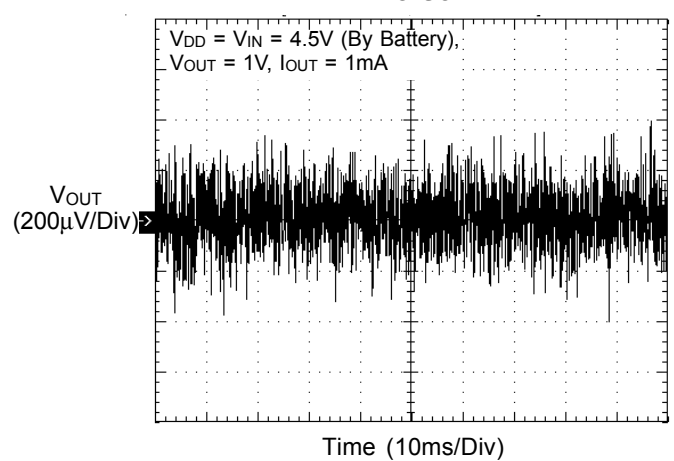
EN Response



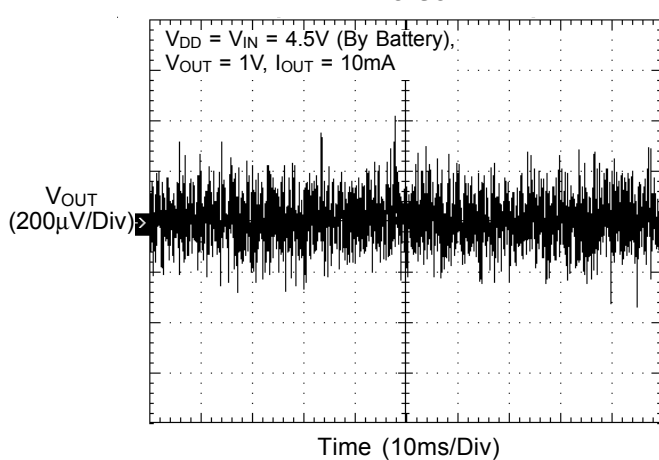
PSRR



Noise



Noise



## Application Information

The RT9041E is a low voltage, low dropout linear regulator with an external bias supply input, capable of supporting an input voltage range from 1V to 5.5V with a fixed output voltage from 1V to 2V in 0.1V increments.

### Supply Voltage Setting

The bias supply voltage ( $V_{DD}$ ) operates from 3V to 5.5V. For better efficiency, it is suggested to operate  $V_{DD}$  at 5V when the output voltage is higher than 1V. Figure 1 shows the curves of the recommended  $V_{DD} - V_{OUT}$  range vs. the dropout voltage ( $V_{IN} - V_{OUT}$ ) values.

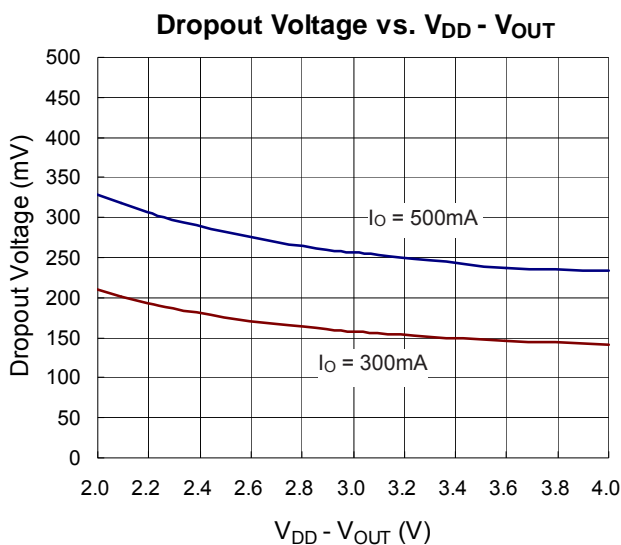


Figure 1. Dropout Voltage vs.  $V_{DD} - V_{OUT}$

### Output Voltage Setting

The RT9041E output voltage is also adjustable from 0.8V to 2.5V via the external resistive voltage divider. The voltage divider resistors can have values up to 800k $\Omega$  because of the very high impedance and low bias current of the sense comparator. The output voltage is set according to the following equation :

$$V_{OUT} = V_{REF} \times \left( 1 + \frac{R1}{R2} \right)$$

where  $V_{REF}$  is the reference voltage with a typical value of 0.8V.

### Chip Enable Operation

The RT9041E goes into sleep mode when the EN pin is in a logic low condition. In this condition, the pass transistor, error amplifier, and band gap are all turned off, reducing the supply current to 1 $\mu$ A (typ.). The EN pin can be directly tied to  $V_{IN}$  to keep the part on.

### Current Limit

The RT9041E contains an independent current limit circuitry, which monitors and controls the pass transistor's gate voltage, limiting the output current to 0.7A (typ.).

### CIN and COUT Selection

Like any low dropout regulator, the external capacitors of the RT9041E must be carefully selected for regulator stability and performance. Using a capacitor of at least 10 $\mu$ F is suitable. The input capacitor must be located at a distance of not more than 0.5 inch from the input pin of the IC. Any good quality ceramic capacitor can be used. However, a capacitor with larger value and lower ESR (Equivalent Series Resistance) is recommended since it will provide better PSRR and line transient response.

The RT9041E is designed specifically to work with low ESR ceramic output capacitor for space saving and performance consideration. Using a ceramic capacitor with value at least 10 $\mu$ F and ESR larger than 40m $\Omega$  on the RT9041E output ensures stability. Nevertheless, the RT9041E can still work well with other types of output capacitors due to its wide range of stable ESR. Figure 2 shows the allowable ESR range as a function of load current for various output capacitance. Output capacitors with larger capacitance can reduce noise and improve load transient response, stability, and PSRR. The output capacitor should be located at a distance of not more than 0.5 inch from the output pin of the RT9041E.

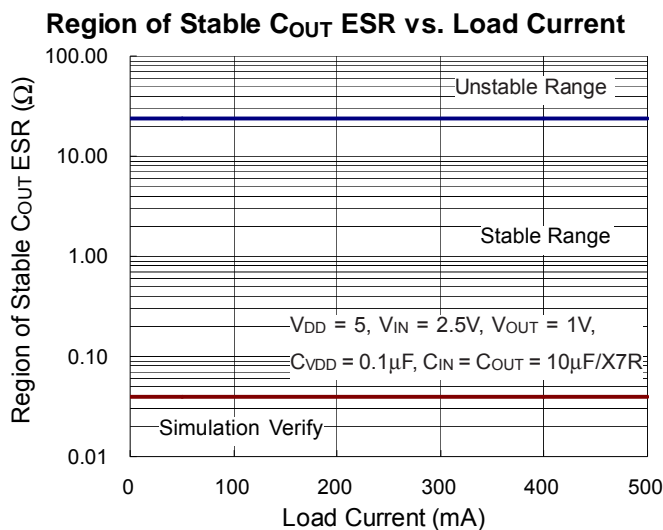


Figure 2. Region of Stable C<sub>OUT</sub> ESR vs. the Load Current

## Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where T<sub>J(MAX)</sub> is the maximum junction temperature, T<sub>A</sub> is the ambient temperature, and θ<sub>JA</sub> is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ<sub>JA</sub>, is layout dependent. For WDFN-8L 2x2 packages, the thermal resistance, θ<sub>JA</sub>, is 120°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T<sub>A</sub> = 25°C can be calculated by the following formula :

$$P_{D(MAX)} = (125^{\circ}\text{C} - 25^{\circ}\text{C}) / (120^{\circ}\text{C/W}) = 0.833\text{W for}$$

WDFN-8L 2x2 package

The maximum power dissipation depends on the operating ambient temperature for fixed T<sub>J(MAX)</sub> and thermal resistance, θ<sub>JA</sub>. The derating curve in Figure 3 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

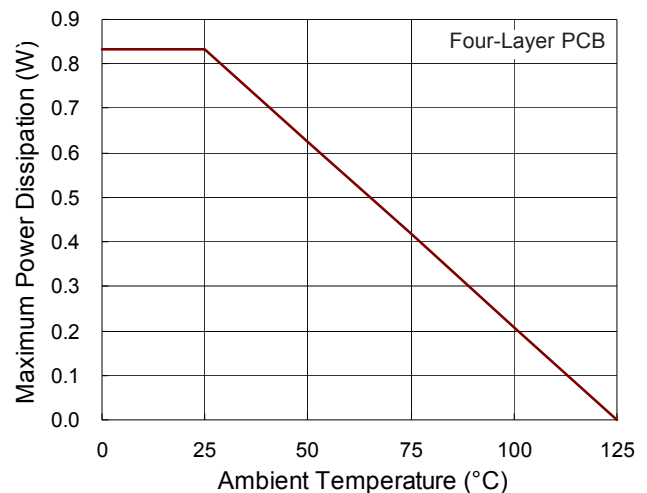
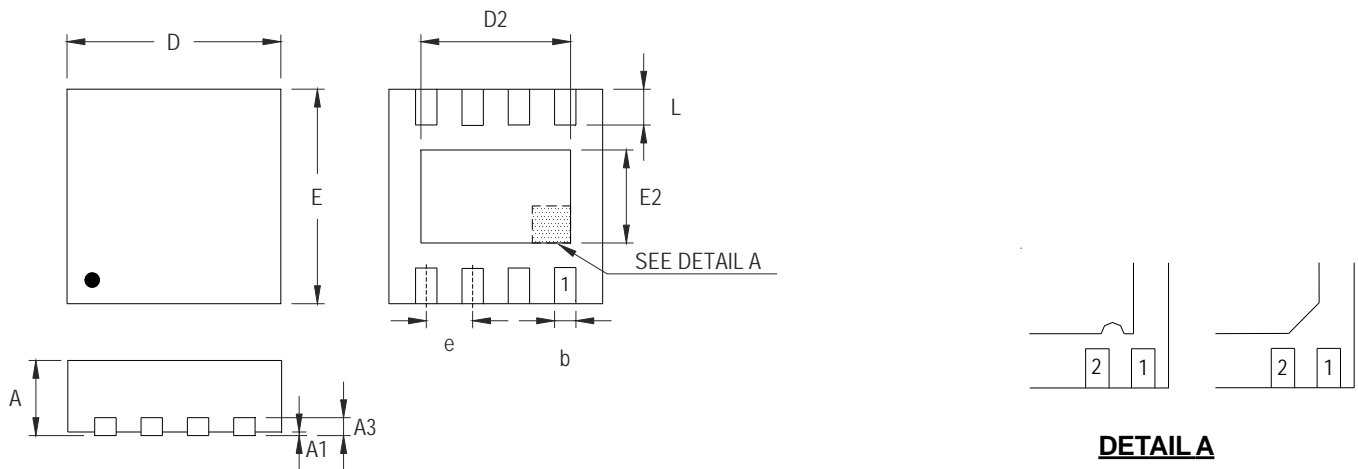


Figure 3. Derating Curve of Maximum Power Dissipation



## Outline Dimension



Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
D	1.950	2.050	0.077	0.081
D2	1.000	1.250	0.039	0.049
E	1.950	2.050	0.077	0.081
E2	0.400	0.650	0.016	0.026
e	0.500		0.020	
L	0.300	0.400	0.012	0.016

**W-Type 8L DFN 2x2 Package**

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