# RT8258

## Table 1. Recommended Component Selection

| $V_{OUT}$ | 1.2V | 1.5V | 1.8V | 2.5V | 3.3V | 5V | 8V | 10V | 15V |
|---|---|---|---|---|---|---|---|---|---|
| R1 (kΩ) | 100 | 91 | 91 | 100 | 100 | 91 | 91 | 91 | 120 |
| R2 (kΩ) | 200 | 100 | 75 | 47 | 32.4 | 17.4 | 10 | 7.87 | 6.8 |
| L (μH) | 3.6 | 3.6 | 4.7 | 6.8 | 10 | 15 | 22 | 22 | 33 |
| $C_{OUT}$(μF) | 22 | 22 | 22 | 22 | 22 | 22 | 22 | 22 | 22 |

Note : The value of R1 is related to the loop bandwidth of the RT8258. It is strongly recommended to follow the parameters in above table for the specific output voltage.

## Function Block Diagram
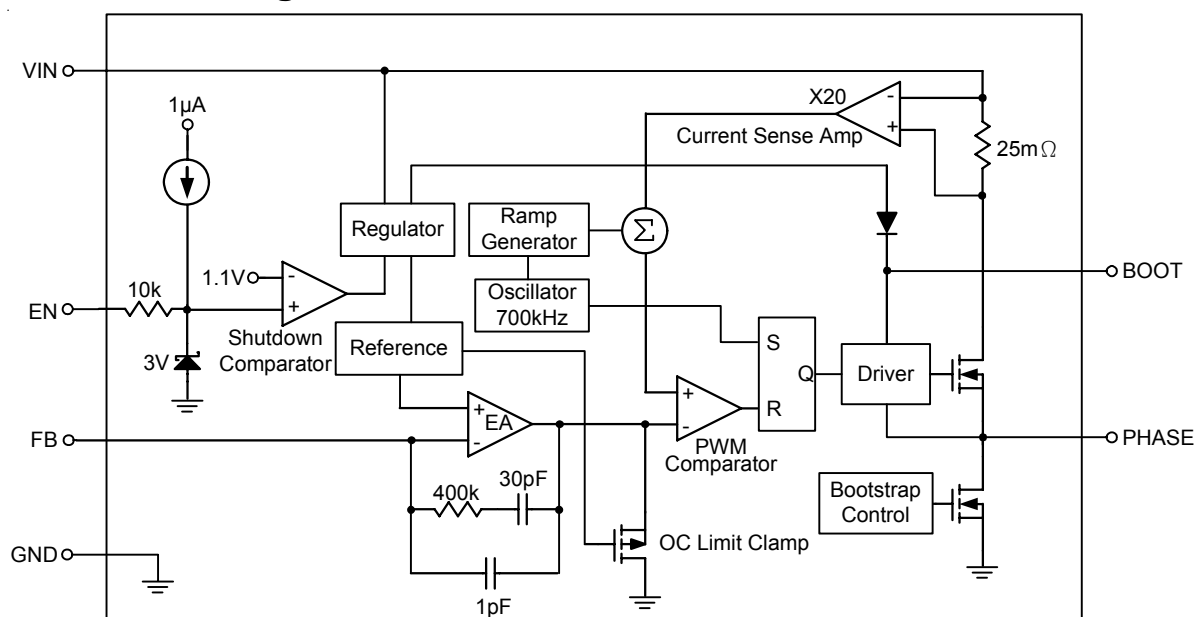


## Functional Pin Description

| Pin No. | Pin Name | Pin Function |
|---|---|---|
| 1 | BOOT | Gate Driver Bootstrap Input Pin. Connect a 10nF or greater capacitor between PHASE and BOOT pins to supply the MOSFET driver. |
| 2 | GND | Ground Pin. This pin should be connected to the (-) terminal of the output capacitor and it should be kept away from the D1 and input capacitor for noise prevention. |
| 3 | FB | Output Voltage Feedback Input Pin. An external resistor divider from the output to GND tapped to the FB pin sets the output voltage. The value of the divider resistors also set loop bandwidth. |
| 4 | EN | Chip Enable (Active High). If the EN pin is open, it will be pulled to high by internal circuit. |
| 5 | VIN | Power Supply Input Pin. Bypass VIN to GND with a suitable large capacitor to prevent large voltage spikes from appearing at the input. |
| 6 | PHASE | Power Switching Output Pin. Connect this pin to the output inductor. |

## Absolute Maximum Ratings    (Note 1)

- Supply Voltage, $V_{IN}$ ------------------------------------------------------------------------ 26V
- PHASE Voltage ------------------------------------------------------------------------ −0.3V to ($V_{IN}$ + 0.3V)
- BOOT Voltage ------------------------------------------------------------------------ $V_{PHASE}$ + 6V
- All Other Pins------------------------------------------------------------------------ 0.3V to 6V
- Power Dissipation, $P_D$ @ $T_A$ = 25°C
  - T/SOT-23-6 ------------------------------------------------------------------------ 0.4W
- Package Thermal Resistance  (Note 2)
  - T/SOT-23-6, $\theta_{JA}$ ------------------------------------------------------------------------ 250°C/W
- Junction Temperature ------------------------------------------------------------------------ 150°C
- Lead Temperature (Soldering, 10 sec.) ------------------------------------------------------------------------ 260°C
- Storage Temperature Range ------------------------------------------------------------------------ −65°C to 150°C
- ESD Susceptibility   (Note 3)
  - HBM (Human Body Mode) ------------------------------------------------------------------------ 2kV
  - MM (Machine Mode) ------------------------------------------------------------------------ 200V

## Recommended Operating Conditions    (Note 4)

- Supply Voltage, $V_{IN}$ ------------------------------------------------------------------------ 4.5V to 24V
- Output Voltage, $V_{OUT}$ ------------------------------------------------------------------------ 0.8V to 15V
- EN Voltage, $V_{EN}$ ------------------------------------------------------------------------ 0V to 5.5V
- Junction Temperature Range ------------------------------------------------------------------------ −40°C to 125°C
- Ambient Temperature Range ------------------------------------------------------------------------ −40°C to 85°C

## Electrical Characteristics
($V_{IN}$ = 12V, $T_A$ = 25°C unless otherwise specified)

| Parameter | | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Feedback Reference Voltage | | $V_{FB}$ | 4.5V ≤ $V_{IN}$ ≤ 24V | 0.784 | 0.8 | 0.816 | V |
| Feedback Current | | $I_{FB}$ | $V_{FB}$ = 0.8V | -- | 0.1 | 0.3 | μA |
| Switch On Resistance | | $R_{DS(ON)}$ | | -- | 0.3 | -- | Ω |
| Switch Leakage | | | $V_{EN}$ = 0V, $V_{PHASE}$ = 0V | -- | -- | 10 | μA |
| Current Limit | | $I_{LIM}$ | $V_{BOOT}$ − $V_{PHASE}$ = 4.8V | 1.6 | 2.1 | -- | A |
| Oscillator Frequency | | $f_{SW}$ | | 600 | 700 | 800 | kHz |
| Maximum Duty Cycle | | | | -- | 90 | -- | % |
| Minimum On-Time | | $t_{ON}$ | | -- | 100 | -- | ns |
| Under Voltage Lockout Threshold Voltage | | | Rising | 3.9 | 4.2 | 4.5 | V |
| Under Voltage Lockout Threshold Hysteresis | | | | -- | 270 | -- | mV |
| EN Input Voltage | Logic High | | | 1.4 | -- | -- | V |
| | Logic Low | | | -- | -- | 0.4 | |
| EN Pull Up Current | | | $V_{EN}$ = 0V | -- | 1 | -- | μA |
| Shutdown Current | | $I_{SHDN}$ | $V_{EN}$ = 0V | -- | 25 | -- | μA |
| Quiescent Current | | $I_Q$ | $V_{EN}$ = 2V, $V_{FB}$ = 1V (No Switching) | -- | 0.55 | 1 | mA |
| Thermal Shutdown | | $T_{SD}$ | | -- | 150 | -- | °C |

**Note 1.** Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

**Note 2.** $\theta_{JA}$ is measured in the natural convection at $T_A = 25°C$ on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

**Note 3.** Devices are ESD sensitive. Handling precaution is recommended.

**Note 4.** The device is not guaranteed to function outside its operating conditions.

# Typical Operating Characteristics

**Efficiency vs. Output Current**



$V_{IN}$ = 24V
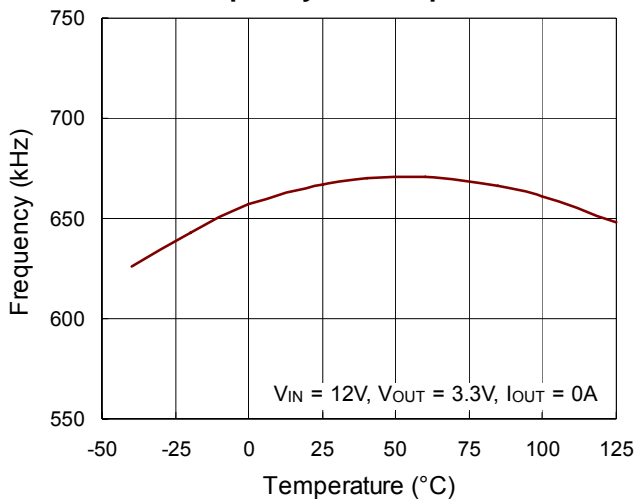$V_{IN}$ = 12V
$V_{OUT}$ = 5V

**Efficiency vs. Output Current**



$V_{IN}$ = 12V
$V_{IN}$ = 24V
$V_{OUT}$ = 3.3V
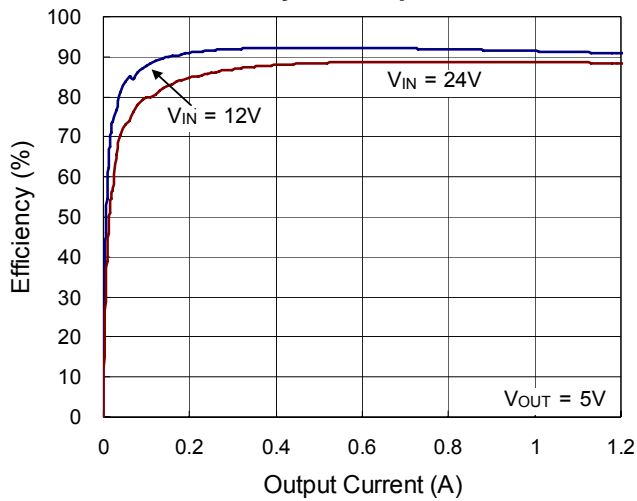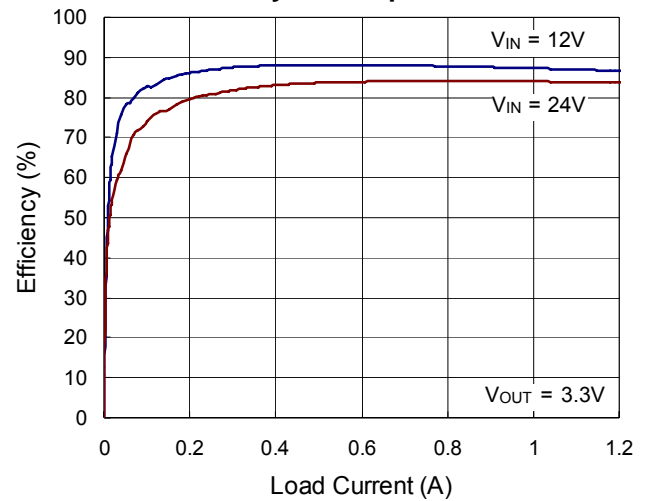
**Output Voltage vs. Output Current**



$V_{IN}$ = 24V
$V_{IN}$ = 12V
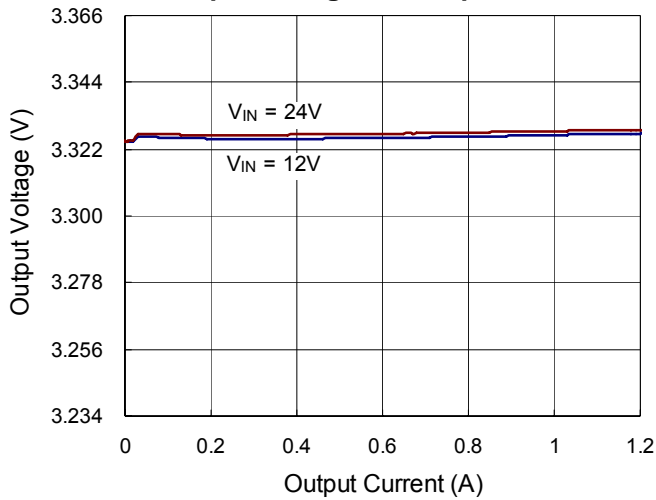
**Output Voltage vs. Temperature**



$V_{IN}$ = 12V
$V_{IN}$ = 24V
$I_{OUT}$ = 0A
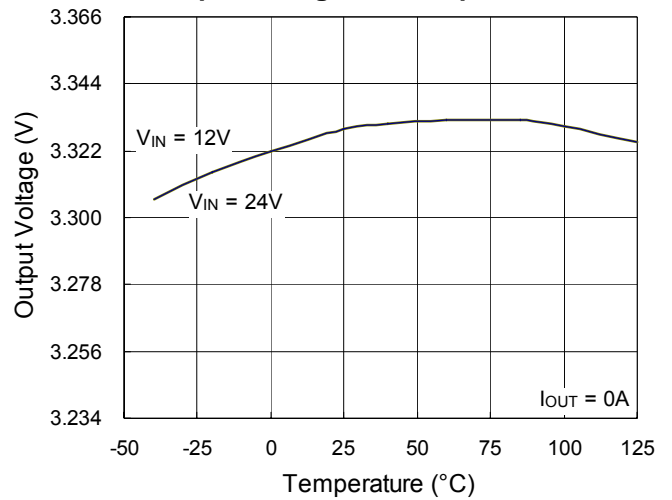
**Frequency vs. Temperature**



$V_{IN}$ = 12V, $V_{OUT}$ = 3.3V, $I_{OUT}$ = 0A

**Quiescent Current vs. Temperature**
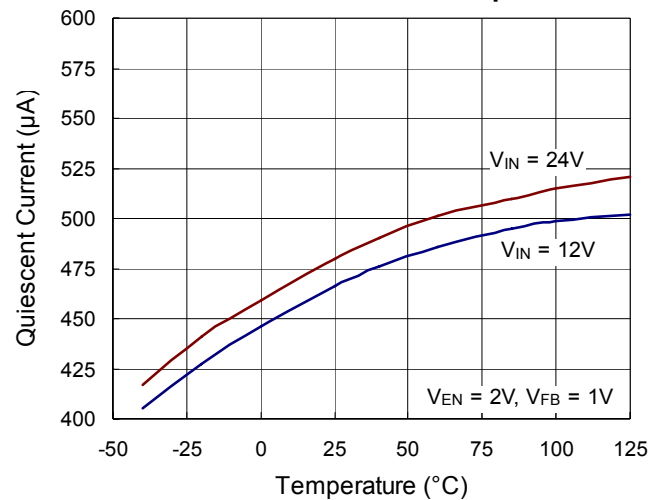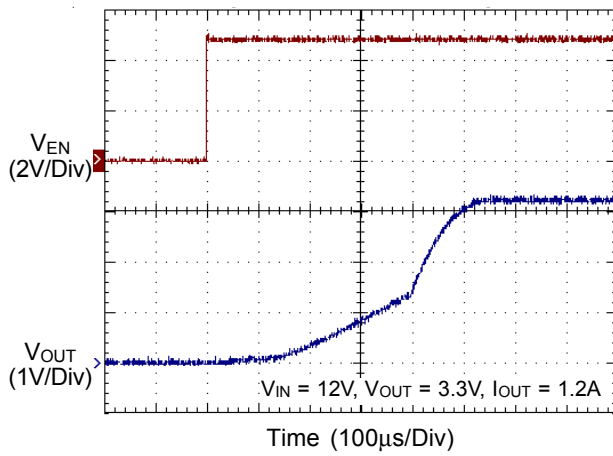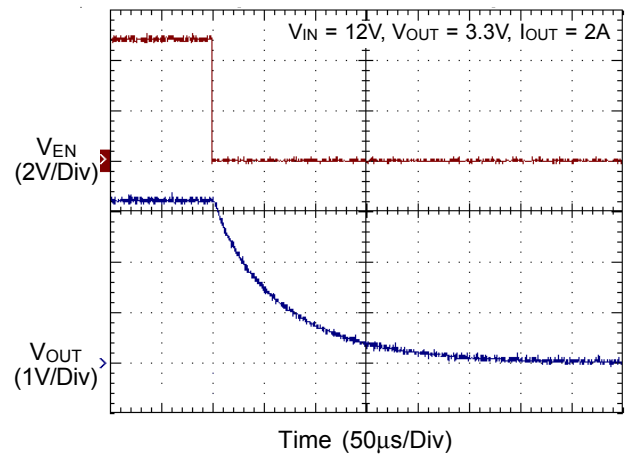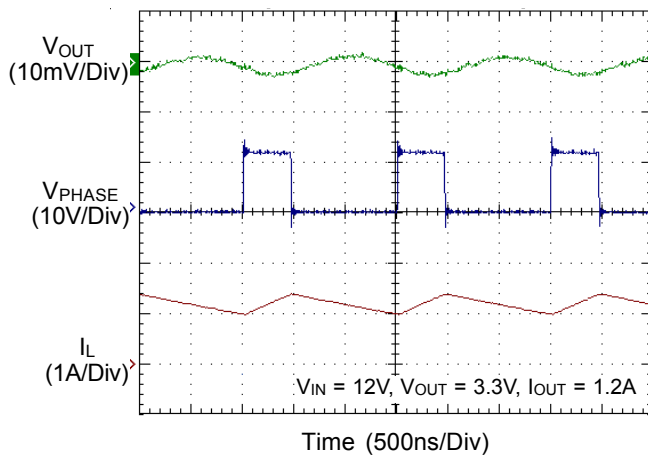


$V_{IN}$ = 24V
$V_{IN}$ = 12V
$V_{EN}$ = 2V, $V_{FB}$ = 1V

**Power On from EN**



$V_{EN}$
(2V/Div)

$V_{OUT}$
(1V/Div)

$V_{IN}$ = 12V, $V_{OUT}$ = 3.3V, $I_{OUT}$ = 1.2A

Time (100μs/Div)

**Power Off from EN**



$V_{IN}$ = 12V, $V_{OUT}$ = 3.3V, $I_{OUT}$ = 2A

$V_{EN}$
(2V/Div)

$V_{OUT}$
(1V/Div)

Time (50μs/Div)

**Output Ripple Voltage**



$V_{OUT}$
(10mV/Div)

$V_{PHASE}$
(10V/Div)

$I_L$
(1A/Div)

$V_{IN}$ = 12V, $V_{OUT}$ = 3.3V, $I_{OUT}$ = 1.2A

Time (500ns/Div)

**Output Ripple Voltage**



$V_{OUT}$
(10mV/Div)

$V_{PHASE}$
(10V/Div)

$I_L$
(1A/Div)

$V_{IN}$ = 24V, $V_{OUT}$ = 3.3V, $I_{OUT}$ = 1.2A

Time (500ns/Div)

**Load Transient Response**



$V_{OUT}$
(0.1V/Div)

$I_{OUT}$
(0.5A/Div)

$V_{IN}$ = 12V, $V_{OUT}$ = 3.3V, $I_{OUT}$ = 0.6A to 1.2A

Time (50μs/Div)

**Load Transient Response**



$V_{OUT}$
(0.1V/Div)

$I_{OUT}$
(0.5A/Div)

$V_{IN}$ = 12V, $V_{OUT}$ = 3.3V, $I_{OUT}$ = 0A to 1.2A

Time (250μs/Div)
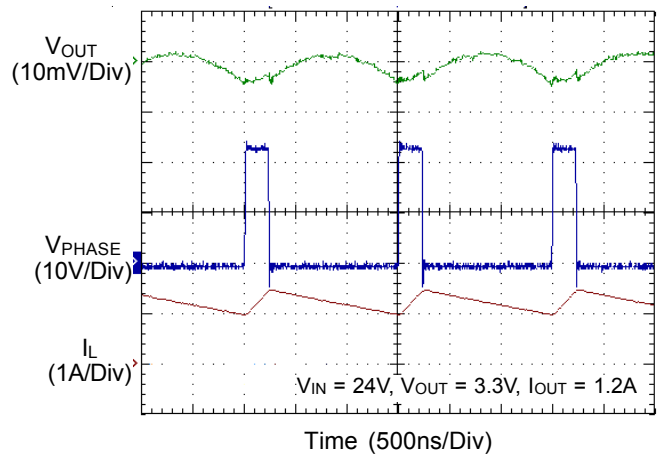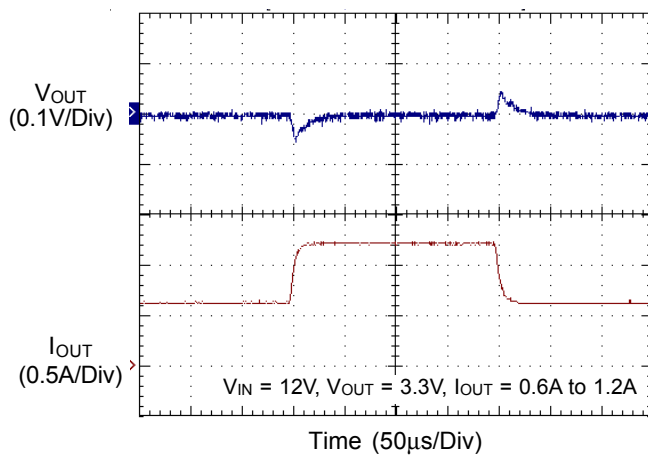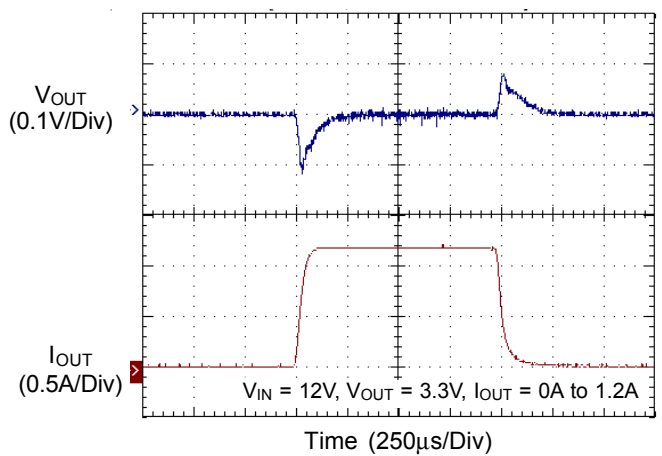
## Application Information

The RT8258 is an asynchronous high voltage buck converter that can support the input voltage range from 4.5V to 24V and the output current can be up to 1.2A.

### Output Voltage Setting

The resistive voltage divider allows the FB pin to sense a fraction of the output voltage as shown in Figure 1.
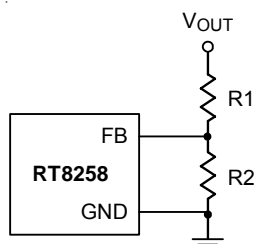


Figure 1. Output Voltage Setting

For adjustable voltage mode, the output voltage is set by an external resistive voltage divider according to the following equation :

$$V_{OUT} = V_{FB}\left(1 + \frac{R1}{R2}\right)$$

Where $V_{FB}$ is the feedback reference voltage (0.8V typ.).

### External Bootstrap Diode

Connect a 10nF low ESR ceramic capacitor between the BOOT pin and PHASE pin. This capacitor provides the gate driver voltage for the high side MOSFET.

It is recommended to add an external bootstrap diode between an external 5V and the BOOT pin for efficiency improvement when input voltage is lower than 5.5V or duty ratio is higher than 65%. The bootstrap diode can be a low cost one such as 1N4148 or BAT54.

The external 5V can be a 5V fixed input from system or a 5V output of the RT8268.
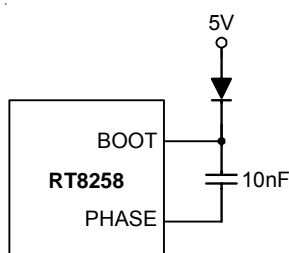


Figure 2. External Bootstrap Diode

### Inductor Selection

The inductor value and operating frequency determine the ripple current according to a specific input and output voltage. The ripple current $\Delta I_L$ increases with higher $V_{IN}$ and decreases with higher inductance.

$$\Delta I_L = \left[\frac{V_{OUT}}{f \times L}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

Having a lower ripple current reduces not only the ESR losses in the output capacitors but also the output voltage ripple. High frequency with small ripple current can achieve highest efficiency operation. However, it requires a large inductor to achieve this goal.

For the ripple current selection, the value of $\Delta I_L = 0.34(I_{MAX})$ will be a reasonable starting point. The largest ripple current occurs at the highest $V_{IN}$. To guarantee that the ripple current stays below the specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left[\frac{V_{OUT}}{f \times \Delta I_{L(MAX)}}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right]$$

### Inductor Core Selection

The inductor type must be selected once the value for L is known. Generally speaking, high efficiency converters can not afford the core loss found in low cost powdered iron cores. So, the more expensive ferrite or mollypermalloy cores will be a better choice.

The selected inductance rather than the core size for a fixed inductor value is the key for actual core loss. As the inductance increases, core losses decrease. Unfortunately, increase of the inductance requires more turns of wire and therefore the copper losses will increase.

Ferrite designs are preferred at high switching frequency due to the characteristics of very low core losses. So, design goals can focus on the reduction of copper loss and the saturation prevention.

Ferrite core material saturates "hard", which means that inductance collapses abruptly when the peak design current is exceeded. The previous situation results in an abrupt increase in inductor ripple current and consequent output voltage ripple.

Do not allow the core to saturate!

Different core materials and shapes will change the size/current and price/current relationship of an inductor.

Toroid or shielded pot cores in ferrite or permalloy materials are small and do not radiate energy. However, they are usually more expensive than the similar powdered iron inductors. The rule for inductor choice mainly depends on the price vs. size requirement and any radiated field/EMI requirements.

**Diode Selection**

When the power switch turns off, the path for the current is through the diode connected between the switch output and ground. This forward biased diode must have a minimum voltage drop and recovery times. Schottky diode is recommended and it should be able to handle those current. The reverse voltage rating of the diode should be greater than the maximum input voltage, and current rating should be greater than the maximum load current. For more detail, please refer to Table 3.

**$C_{IN}$ and $C_{OUT}$ Selection**

The input capacitance, $C_{IN,}$ is needed to filter the trapezoidal current at the source of the top MOSFET. To prevent large ripple current, a low ESR input capacitor sized for the maximum RMS current should be used. The RMS current is given by :

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief.

Choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design.

The selection of $C_{OUT}$ is determined by the required Effective Series Resistance (ESR) to minimize voltage ripple.

Moreover, the amount of bulk capacitance is also a key for $C_{OUT}$ selection to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section.

The output ripple, $\Delta V_{OUT}$, is determined by :

$$\Delta V_{OUT} \leq \Delta I_L \left[ ESR + \frac{1}{8fC_{OUT}} \right]$$

The output ripple will be highest at the maximum input voltage since $\Delta I_L$ increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirement. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR value. However, it provides lower capacitance density than other types. Although Tantalum capacitors have the highest capacitance density, it is important to only use types that pass the surge test for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR. However, it can be used in cost-sensitive applications for ripple current rating and long term reliability considerations. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing.

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, $V_{IN}$. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at $V_{IN}$ large enough to damage the part.

**Checking Transient Response**

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, $V_{OUT}$ immediately shifts by an amount equal to $\Delta I_{LOAD}$ (ESR) and also begins to charge or discharge $C_{OUT}$ generating a feedback error signal for the regulator to return $V_{OUT}$ to its steady-state value. During this recovery time, $V_{OUT}$ can be monitored for overshoot or ringing that would indicate a stability problem.

## Thermal Considerations

For continuous operation, do not exceed the maximum operation junction temperature 125°C. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum operation junction temperature, $T_A$ is the ambient temperature and the $\theta_{JA}$ is the junction to ambient thermal resistance.

For recommended operating conditions specification of the RT8258, the maximum junction temperature of the die is 125°C. The junction to ambient thermal resistance $\theta_{JA}$ is layout dependent. For T/SOT-23-6 package, the thermal resistance $\theta_{JA}$ is 250°C/W on standard JEDEC 51-3 single layer thermal test board. The maximum power dissipation at $T_A$ = 25°C can be calculated by following formula :

$$P_{D(MAX)} = (125°C - 25°C) / (250°C/W) = 0.4W \text{ for}$$
T/SOT-23-6 package

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance $\theta_{JA}$ . For RT8258 package, the Figure 3 of derating curve allows the designer to see the effect of rising ambient temperature on the maximum power dissipation allowed.
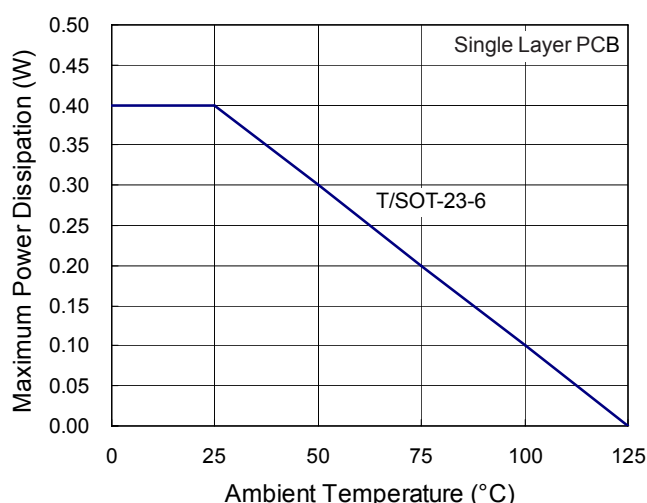
## Layout Consideration

Follow the PCB layout guidelines for optimal performance of RT8258.

‣ Keep the traces of the main current paths as short and wide as possible.

‣ Put the input capacitor as close as possible to the device pins (VIN and GND).

‣ PHASE node is with high frequency voltage swing and should be kept at small area. Keep sensitive components away from the PHASE node to prevent stray capacitive noise pick-up.

‣ Place the feedback components to the FB pin as close as possible.

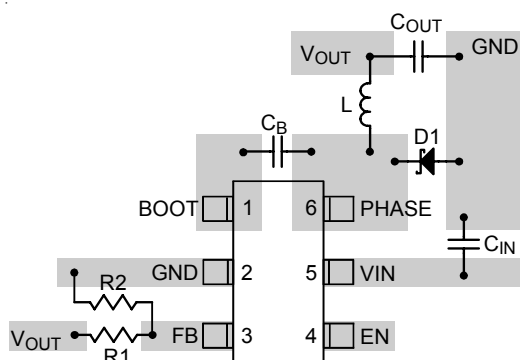‣ Connect the GND to a ground plane for noise reduction and thermal dissipation.



Figure 4. PCB Layout Guide



Figure 3. Derating Curve for RT8258 Package

**Table 2. Suggested Inductors for L**

| Component Supplier | Series | Dimensions (mm) |
|---|---|---|
| TDK | SLF12555T | 12.5x12.5x5.5 |
| TAIYO YUDEN | NR8040 | 8x8x4 |
| TDK | SLF12565T | 12.5x12.5x6.5 |

**Table 3. Suggested Capacitors for $C_{IN}$ and $C_{OUT}$**

| Location | Component Supplier | Part No. | Capacitance ($\mu$F) | Case Size |
|---|---|---|---|---|
| $C_{IN}$ | MURATA | GRM31CR61E106K | 10 | 1206 |
| $C_{IN}$ | TDK | C3225X5R1E106K | 10 | 1206 |
| $C_{IN}$ | TAIYO YUDEN | TMK316BJ106ML | 10 | 1206 |
| $C_{OUT}$ | MURATA | GRM31CR61C226M | 22 | 1206 |
| $C_{OUT}$ | TDK | C3225X5R1C226M | 22 | 1206 |
| $C_{OUT}$ | TAIYO YUDEN | EMK316BJ226ML | 22 | 1206 |

**Table 4. Suggested Diode for D1**

| Component Supplier | Series | $V_{RRM}$ (V) | $I_{OUT}$ (A) | Package |
|---|---|---|---|---|
| DIODES | B230A | 30 | 2 | DO-214AC |
| DIODES | B330A | 30 | 3 | DO-214AC |
| PANJIT | SK23 | 30 | 2 | DO-214AC |
| PANJIT | SK33 | 30 | 3 | DO-214AB |

## Outline Dimension
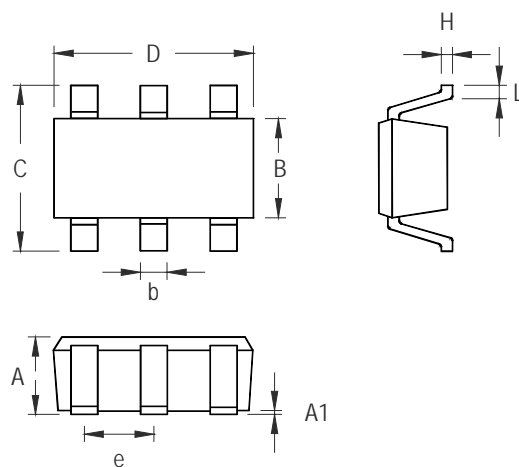


| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|--------|------|------|------|------|
| | **Min** | **Max** | **Min** | **Max** |
| A | 0.889 | 1.295 | 0.031 | 0.051 |
| A1 | 0.000 | 0.152 | 0.000 | 0.006 |
| B | 1.397 | 1.803 | 0.055 | 0.071 |
| b | 0.250 | 0.560 | 0.010 | 0.022 |
| C | 2.591 | 2.997 | 0.102 | 0.118 |
| D | 2.692 | 3.099 | 0.106 | 0.122 |
| e | 0.838 | 1.041 | 0.033 | 0.041 |
| H | 0.080 | 0.254 | 0.003 | 0.010 |
| L | 0.300 | 0.610 | 0.012 | 0.024 |

**SOT-23-6 Surface Mount Package**
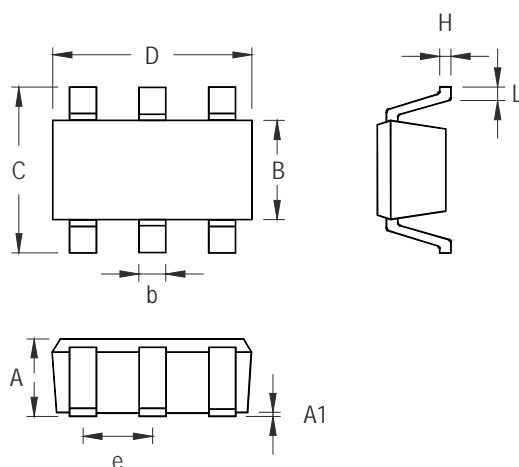
| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|--------|------|------|------|------|
| | Min | Max | Min | Max |
| A | 0.700 | 1.000 | 0.028 | 0.039 |
| A1 | 0.000 | 0.100 | 0.000 | 0.004 |
| B | 1.397 | 1.803 | 0.055 | 0.071 |
| b | 0.300 | 0.559 | 0.012 | 0.022 |
| C | 2.591 | 3.000 | 0.102 | 0.118 |
| D | 2.692 | 3.099 | 0.106 | 0.122 |
| e | 0.838 | 1.041 | 0.033 | 0.041 |
| H | 0.080 | 0.254 | 0.003 | 0.010 |
| L | 0.300 | 0.610 | 0.012 | 0.024 |

**TSOT-23-6 Surface Mount Package**

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