

P3P623S05A/B, P3P623S09A/B

BLOCK DIAGRAM

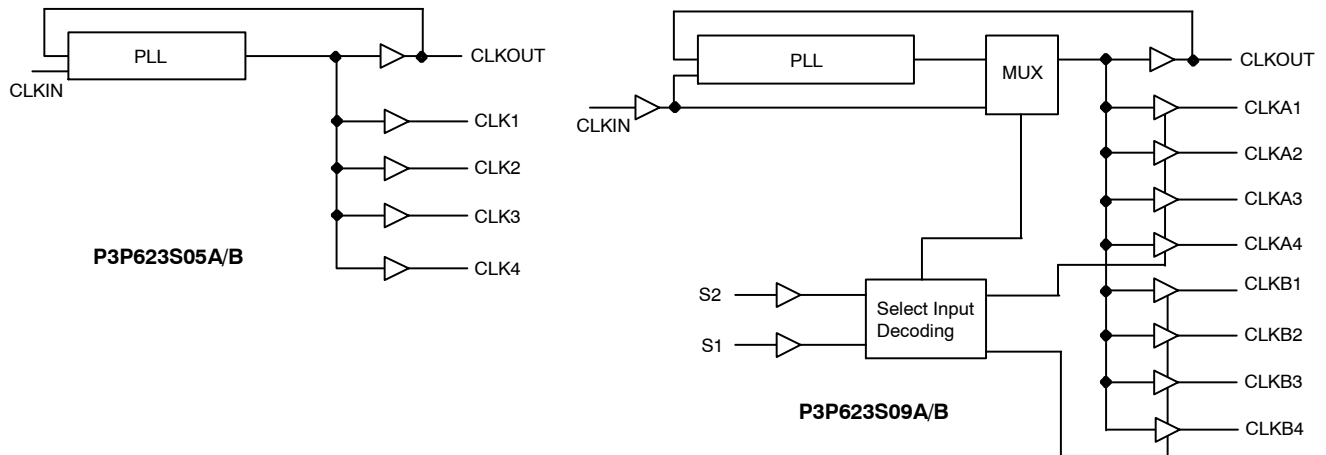


Figure 1. General Block Diagram

PIN CONFIGURATION

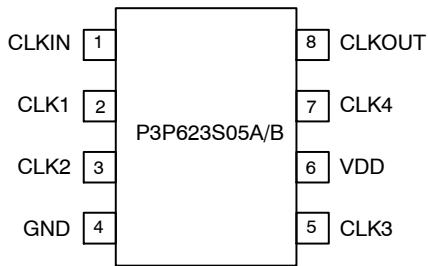


Figure 2. Pin Configuration for P3P623S05A/B

Table 1. PIN DESCRIPTION FOR P3P623S05A/B

| Pin # | Pin Name | Type | Description |
|-------|-----------------|------|---|
| 1 | CLKIN (Note 1) | I | External reference Clock input, 5 V tolerant input. |
| 2 | CLK1 (Note 2) | O | Buffered clock output (Note 3) |
| 3 | CLK2 (Note 2) | O | Buffered clock output (Note 3) |
| 4 | GND | P | Ground |
| 5 | CLK3 (Note 2) | O | Buffered clock output (Note 3) |
| 6 | VDD | P | 3.3 V supply |
| 7 | CLK4 (Note 2) | O | Buffered clock output (Note 3) |
| 8 | CLKOUT (Note 3) | O | Buffered clock output. Internal feedback on this pin. |

1. Weak pull-down
2. Weak pull-down on all outputs
3. Buffered clock output is Timing-Safe

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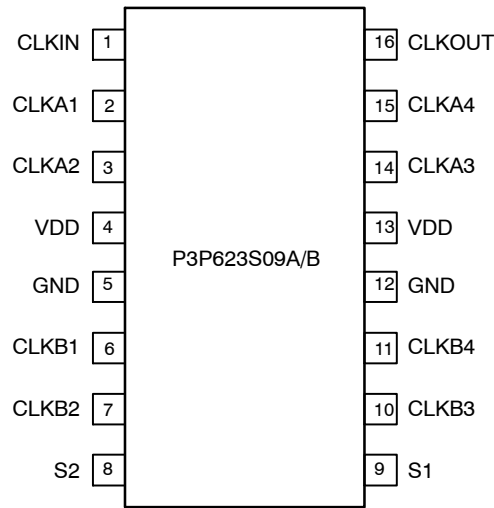


Figure 3. Pin Configuration for P3P623S09A/B

Table 2. PIN DESCRIPTION FOR P3P623S05A/B

| Pin # | Pin Name | Type | Description |
|-------|-----------------|------|---|
| 1 | CLKIN (Note 1) | I | External reference Clock input, 5 V tolerant input. |
| 2 | CLKA1 (Note 2) | O | Buffered clock Bank A output (Note 4) |
| 3 | CLKA2 (Note 2) | O | Buffered clock Bank A output (Note 4) |
| 4 | VDD | P | 3.3 V supply |
| 5 | GND | P | Ground |
| 6 | CLKB1 (Note 2) | O | Buffered clock Bank B output (Note 4) |
| 7 | CLKB2 (Note 2) | O | Buffered clock Bank B output (Note 4) |
| 8 | S2 (Note 3) | I | Select input, bit 2. See Select Input Decoding table for P3P623S09A/B for more details. |
| 9 | S1 (Note 3) | I | Select input, bit 1. See Select Input Decoding table for P3P623S09A/B for more details. |
| 10 | CLKB3 (Note 2) | O | Buffered clock Bank B output (Note 4) |
| 11 | CLKB4 (Note 2) | O | Buffered clock Bank B output (Note 4) |
| 12 | GND | P | Ground |
| 13 | VDD | P | 3.3 V supply |
| 14 | CLKA3 (Note 2) | O | Buffered clock Bank A output (Note 4) |
| 15 | CLKA4 (Note 2) | O | Buffered clock Bank A output (Note 4) |
| 16 | CLKOUT (Note 2) | O | Buffered clock output. Internal feedback on this pin. |

1. Weak pull-down
2. Weak pull-down on all outputs
3. Weak pull-up on these inputs
4. Buffered clock output is Timing-Safe

Table 3. SELECT INPUT DECODING TABLE FOR P3P623S09A/B

| S2 | S1 | CLK A1 – A4 | CLK B1 – B4 | CLKOUT (Note 5) | Output Source | PLL Shut-Down |
|----|----|-------------|-------------|-----------------|---------------|---------------|
| 0 | 0 | Three-state | Three-state | Driven | PLL | N |
| 0 | 1 | Driven | Three-state | Driven | PLL | N |
| 1 | 0 | Driven | Driven | Driven | Reference | Y |
| 1 | 1 | Driven | Driven | Driven | PLL | N |

5. This output is driven and has an internal feedback for the PLL. The load on this output can be adjusted to change the skew between the reference and the Output.

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Table 4. SPREAD SPECTRUM CONTROL AND INPUT-OUTPUT SKEW TABLE

| Frequency (MHz) | Device | Deviation | Input-Output Skew ($\pm T_{SKEW}$) |
|-----------------|------------------|--------------|--------------------------------------|
| 32 | P3P623S05A / 09A | $\pm 0.25\%$ | 0.125 |
| | P3P623S05B / 09B | $\pm 0.50\%$ | 0.25 |

NOTE: T_{SKEW} is measured in units of the Clock Period

Table 5. ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Rating | Unit |
|------------------|---|--------------|------|
| VDD | Supply Voltage to Ground Potential | -0.5 to +4.6 | V |
| VIN | DC Input Voltage (CLKIN) | -0.5 to +7 | |
| T _{STG} | Storage temperature | -65 to +125 | °C |
| T _s | Max. Soldering Temperature (10 sec) | 260 | °C |
| T _J | Junction Temperature | 150 | °C |
| T _{DV} | Static Discharge Voltage (As per JEDEC STD22- A114-B) | 2 | KV |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 6. OPERATING CONDITIONS

| Parameter | Description | Min | Max | Unit |
|-----------------|---|-----|-----|------|
| VDD | Supply Voltage | 3.0 | 3.6 | V |
| T _A | Operating Temperature (Ambient Temperature) | -40 | +85 | °C |
| C _L | Load Capacitance | | 30 | pF |
| C _{IN} | Input Capacitance | | 7 | pF |

Table 7. ELECTRICAL CHARACTERISTICS

| Parameter | Description | Test Conditions | Min | Typ | Max | Units |
|-----------------|------------------------------|-----------------------------------|-----|-----|-----|-------|
| V _{IL} | Input LOW Voltage (Note 1) | | | | 0.8 | V |
| V _{IH} | Input HIGH Voltage (Note 1) | | 2.0 | | | V |
| I _{IL} | Input LOW Current | V _{IN} = 0 V | | | 50 | μA |
| I _{IH} | Input HIGH Current | V _{IN} = V _{DD} | | | 100 | μA |
| V _{OL} | Output LOW Voltage (Note 2) | I _{OL} = 8 mA | | | 0.4 | V |
| V _{OH} | Output HIGH Voltage (Note 2) | I _{OH} = -8 mA | 2.4 | | | V |
| I _{DD} | Supply Current | Unloaded outputs | | 15 | | mA |
| Z _O | Output Impedance | | | 23 | | Ω |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. CLKIN input has a threshold voltage of VDD/2

2. Parameter is guaranteed by design and characterization. Not tested in production.

Table 8. SWITCHING CHARACTERISTICS

| Parameter | Description | Test Conditions | Min | Typ | Max | Units |
|------------|---|---|-----|-----|-----------|-------|
| | Input Frequency | | 20 | | 50 | MHz |
| $1/t_1$ | Output Frequency | 30 pF load | 20 | | 50 | MHz |
| t_D | Duty Cycle (Notes 3, 4) = $(t_2/t_1) * 100$ | Measured at $V_{DD}/2$ | 40 | 50 | 60 | % |
| t_3 | Output Rise Time (Notes 3, 4) | Measured between 0.8 V and 2.0 V | | | 2.5 | nS |
| t_4 | Output Fall Time (Notes 3, 4) | Measured between 2.0 V and 0.8 V | | | 2.5 | nS |
| t_5 | Output-to-output skew (Notes 3, 4) | All outputs equally loaded | | | 250 | pS |
| t_6 | Delay, CLKIN Rising Edge to CLKOUT Rising Edge (Note 4) | Measured at $V_{DD}/2$ | | | ± 350 | pS |
| t_7 | Device-to-Device Skew (Note 4) | Measured at $V_{DD}/2$ on the CLKOUT pins of the device | | | 700 | pS |
| t_J | Cycle-to-cycle jitter (Notes 3, 4) | Loaded outputs | | | ± 200 | pS |
| t_{LOCK} | PLL Lock Time (Note 4) | Stable power supply, valid clock presented on CLKIN pin | | | 1.0 | mS |

3. All parameters specified with 30 pF loaded outputs.

4. Parameter is guaranteed by design and characterization. Not tested in production.

Switching Waveforms

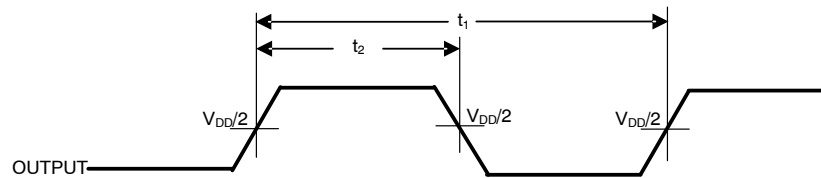


Figure 4. Duty Cycle Timing

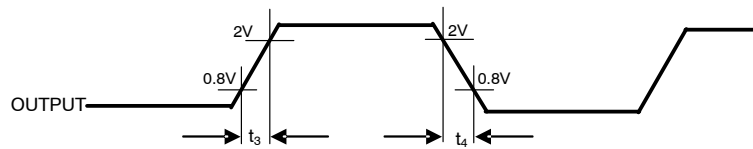


Figure 5. All Outputs Rise/Fall Time

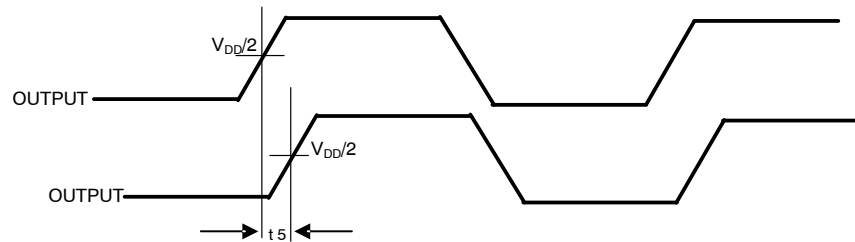


Figure 6. Output-Output Skew

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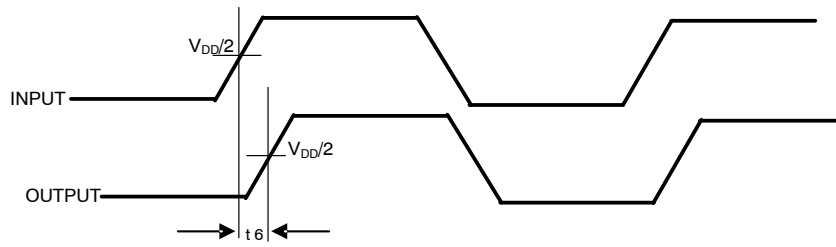


Figure 7. Input-Output Propagation Delay

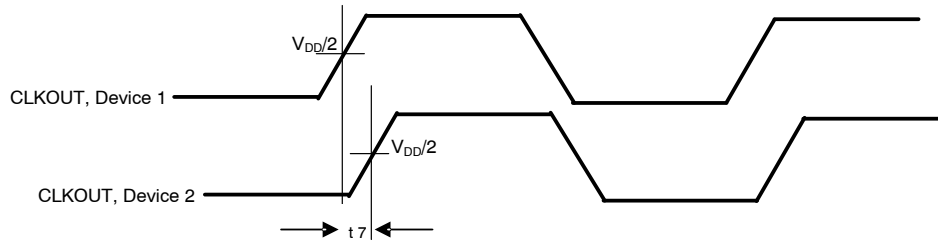


Figure 8. Device-Device Skew

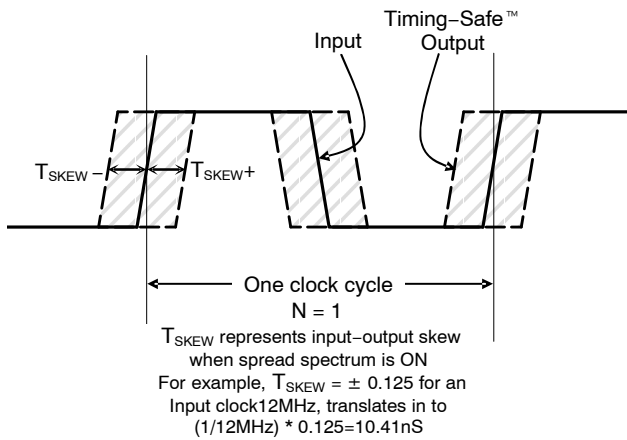


Figure 9. Input-Output Skew

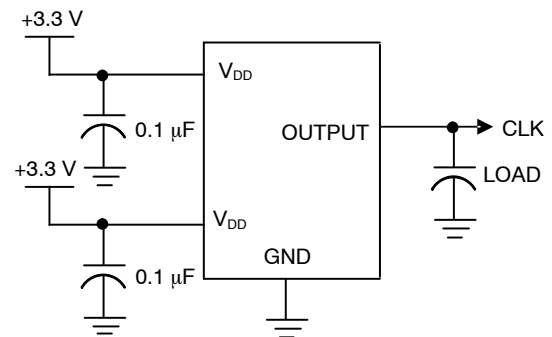


Figure 10. Test Circuit

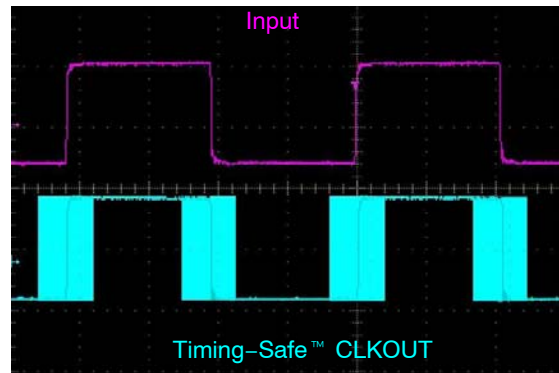
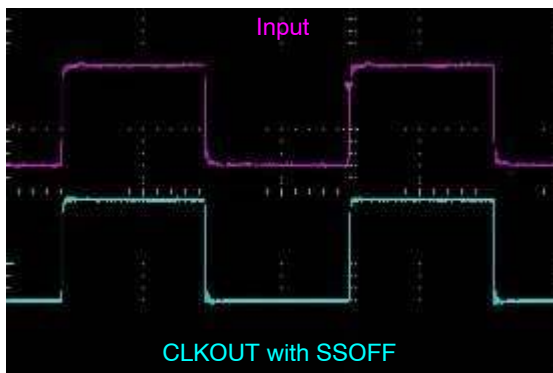


Figure 11. Typical Example of Timing-Safe Waveform

Table 9. ORDERING INFORMATION

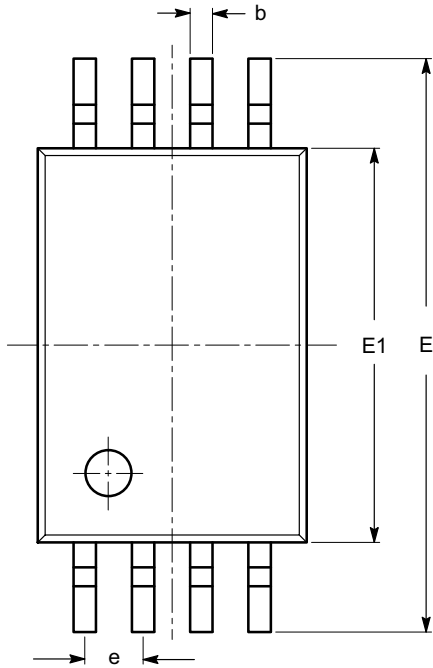
| Part Number | Marking | Package Type | Temperature |
|------------------|---------|---|--------------|
| P3P623S05BG-08TR | ADQ | 8 pin, 4.4 mm TSSOP, Tape & Reel, Green | 0°C to +70°C |

NOTE: A "microdot" placed at the end of last row of marking or just below the last row toward the center of package indicates Pb-free

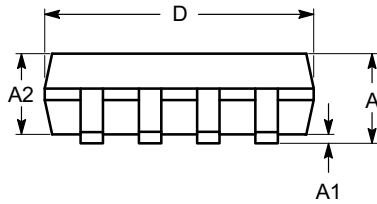
P3P623S05A/B, P3P623S09A/B

PACKAGE DIMENSIONS

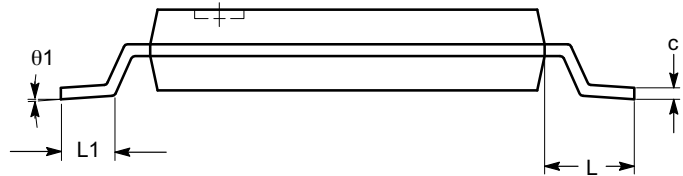
TSSOP8, 4.4x3
CASE 948AL
ISSUE O



TOP VIEW



SIDE VIEW



END VIEW

| SYMBOL | MIN | NOM | MAX |
|----------|----------|------|------|
| A | | | 1.20 |
| A1 | 0.05 | | 0.15 |
| A2 | 0.80 | 0.90 | 1.05 |
| b | 0.19 | | 0.30 |
| c | 0.09 | | 0.20 |
| D | 2.90 | 3.00 | 3.10 |
| E | 6.30 | 6.40 | 6.50 |
| E1 | 4.30 | 4.40 | 4.50 |
| e | 0.65 BSC | | |
| L | 1.00 REF | | |
| L1 | 0.50 | 0.60 | 0.75 |
| θ | 0° | | 8° |

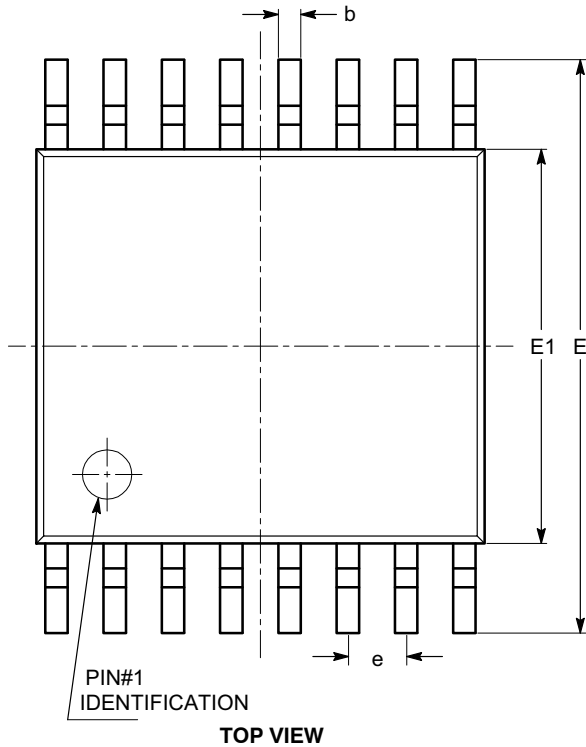
Notes:

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MO-153.

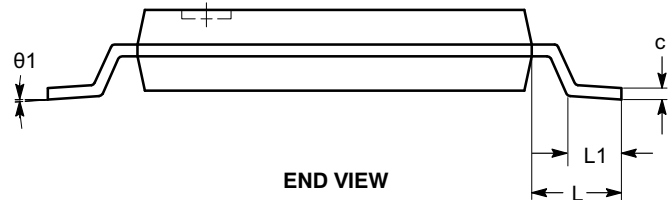
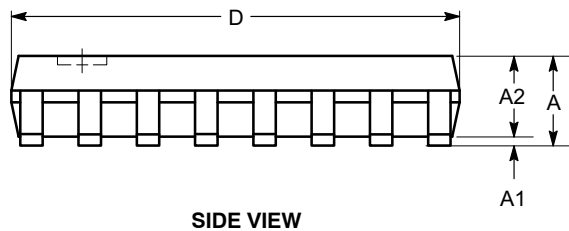
P3P623S05A/B, P3P623S09A/B

PACKAGE DIMENSIONS

TSSOP16, 4.4x5
CASE 948AN
ISSUE O




| SYMBOL | MIN | NOM | MAX |
|--------|----------|-----|------|
| A | | | 1.10 |
| A1 | 0.05 | | 0.15 |
| A2 | 0.85 | | 0.95 |
| b | 0.19 | | 0.30 |
| c | 0.13 | | 0.20 |
| D | 4.90 | | 5.10 |
| E | 6.30 | | 6.50 |
| E1 | 4.30 | | 4.50 |
| e | 0.65 BSC | | |
| L | 1.00 REF | | |
| L1 | 0.45 | | 0.75 |
| θ | 0° | | 8° |



Notes:

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MO-153.

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