FAIRCHILD SEMICONDUCTOR®

September 2013

NC7SV74

TinyLogic® ULP-A D-Type Flip-Flop with Preset and Clear

Features

- Space-saving US8 surface-mount package
- MicroPak™ Pb-free leadless package
- 0.9V to 3.6V V_{CC} supply operation
- 3.6V over-voltage tolerant I/Os at V_{CC} from 0.9V to 3.6V
- Extremely High Speed t_{PD}
  - 1.0 ns typ for 2.7V to 3.6V V_{CC}
  - 1.2 ns typ for 2.3V to 2.7V V_{CC}
  - 1.9 ns typ for 1.65V to 1.95V V_{CC}
  - 3.2 ns typ for 1.4V to 1.6V V_{CC}
  - 6.0 ns typ for 1.1V to 1.3V V_{CC}
  - 13.0 ns typ for 0.9V V_{CC}
- Power-off high-impedance inputs and outputs
- High static drive (I_{OH}/I_{OL})
  - ±24.0 mA @ 3.00V V_{CC}
  - ±18.0 mA @ 2.30V V_{CC}
  - ±6.0 mA @ 1.65V V_{CC}
  - ±4.0 mA @ 1.4V V_{CC}
  - ±2.0 mA @ 1.1V V_{CC}
  - ±0.1 mA @ 0.9V V_{CC}
- Ultra low dynamic power

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General Description

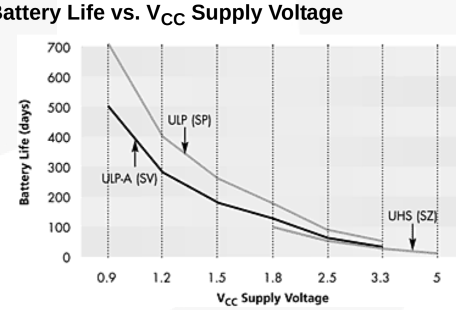
The NC7SV74 is a single D-type CMOS flip-flop with preset and clear from Fairchild's Ultra Low Power-A (ULP-A) series of TinyLogic products, in space-saving US8 and MicroPak™ packages. ULP-A is ideal for applications that require extreme high speed, high drive, and low power.

This product is designed for a wide low-voltage operating range (0.9V to 3.6V V_{CC}) and applications that require more drive and speed than the TinyLogic ULP series, but still require low power consumption.

The NC7SV74 is uniquely designed for optimized power and speed, and is fabricated with an advanced CMOS technology to achieve high-speed operation while maintaining low CMOS power dissipation.

The signal level applied to the D input is transferred to the Q output during the positive-going transition of the CLK pulse.

Battery Life vs. V_{CC} Supply Voltage



TinyLogic ULP and ULP-A with up to 50% less power consumption can extend your battery life significantly.

Battery Life = ($V_{battery}$ *$I_{battery}$*.9)/(P_{device})/24hrs/day

where: $P_{device} = (I_{CC} * V_{CC}) + (C_{PD} + C_L) * V_{CC}^2 * f$

Assumes ideal 3.6V Lithium Ion battery with current rating of 900mAH and derated 90% and device frequency at 10MHz, with C_L = 15 pF load.

Ordering Information

Order Number	Package Number	Product Code Top Mark	Package Description	Supplied As
NC7SV74K8X	MAB08A	V74	8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide	3k Units on Tape and Reel
NC7SV74L8X	MAC08A	Z4	Pb-Free 8-Lead MicroPak, 1.6 mm Wide	5k Units on Tape and Reel

Pb-Free package per JEDEC J-STD-020B.

Pin Descriptions

Pin Names	Description
D	Data Input
CK	Clock Pulse Input
$\overline{CLR}$	Direct Clear Input
Q, $\overline{Q}$	Flip-Flop Output
$\overline{PR}$	Direct Preset Input

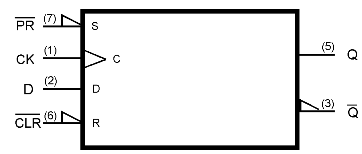
Truth Table/s

Inputs				Outputs		Function
$\overline{CLR}$	$\overline{PR}$	D	CK	Q	$\overline{Q}$	
L	H	X	X	L	H	Clear
H	L	X	X	H	L	Preset
L	L	X	X	H	H	—
H	H	L	-	L	H	—
H	H	H	-	H	L	—
H	H	X	‾	Q_n	$\overline{Q}_n$	No Change

H = HIGH Logic Level
L = LOW Logic Level
Q_n = No change in data
X = Immaterial
Z = High Impedance
- = Rising Edge
‾ = Falling edge

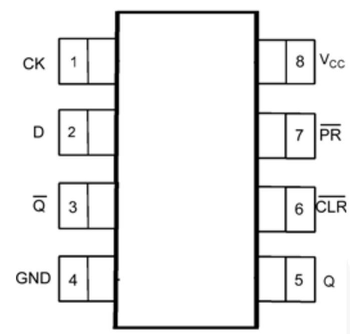
Logic Symbol/s

IEEE/IEC



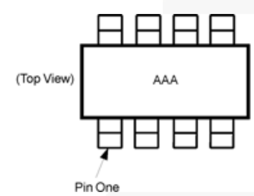
Connection Diagram/s

Pin Assignments for US8



(Top View)

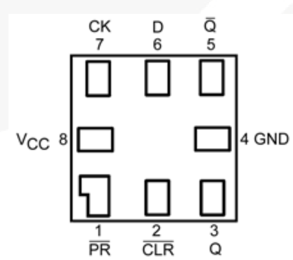
Pin One Orientation Diagram



AAA represents Product Code Top Mark - *see ordering info*

Note: Orientation of Top Mark determines Pin One location. Read the top product code mark left to right, Pin One is the lower left pin (see diagram).

Pad Assignments for MicroPak



(Top Through View)

Absolute Maximum Ratings

Absolute Maximum Ratings: are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The “Recommended Operating Conditions” table will define the conditions for actual device operation. I_O Absolute Maximum Rating must be observed.

Supply Voltage (V_{CC})	-0.5V to +4.6V
DC Input Voltage (V_{IN})	-0.5V to +4.6V
DC Output Voltage (V_{OUT})	
HIGH or LOW State	-0.5V to V_{CC} +0.5V
V_{CC} = 0V	-0.5V to +4.6V
DC Input Diode Current (I_{IK}) V_{IN} < 0V	±50 mA
DC Output Diode Current (I_{OK})	
V_{OUT} < 0V	-50 mA
V_{OUT} > V_{CC}	+50 mA
DC Output Source/Sink Current (I_{OH}/I_{OL})	± 50 mA
DC V_{CC} or Ground Current per	
Supply Pin (I_{CC} or Ground)	± 50 mA
Storage Temperature Range (T_{STG})	-65°C to +150°C

Recommended Operating Conditions

Unused inputs must be held HIGH or LOW. They may not float.

Power Supply	0.9V to 3.6V
Input Voltage (V_{IN})	0V to 3.6V
Output Voltage (V_{OUT})	
V_{CC} = 0.0V	0V to 3.6V
HIGH or LOW State	0V to V_{CC}
Output Current in I_{OH}/I_{OL}	
V_{CC} = 3.0V to 3.6V	±24.0 mA
V_{CC} = 2.3V to 2.7V	±18.0 mA
V_{CC} = 1.65V to 1.95V	±6.0 mA
V_{CC} = 1.4V to 1.6V	±4.0 mA
V_{CC} = 1.1V to 1.3V	±2.0 mA
V_{CC} = 0.9V	±0.1 mA
Free Air Operating Temperature (T_A)	-40°C to +85°C
Minimum Input Edge Rate (dt/dv)	
V_{IN} = 0.8V to 2.0V, V_{CC} = 3.0V	10 ns/V

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$ Min.	$T_A = +25°C$ Max.	$T_A = -40°C$ to $+85°C$ Min.	$T_A = -40°C$ to $+85°C$ Max.	Units	Conditions
V_{IH}	HIGH Level Input Voltage	0.90	$0.65 \times V_{CC}$		$0.65 \times V_{CC}$		V	
		$1.10 \le V_{CC} \le 1.30$	$0.65 \times V_{CC}$		$0.65 \times V_{CC}$			
		$1.40 \le V_{CC} \le 1.60$	$0.65 \times V_{CC}$		$0.65 \times V_{CC}$			
		$1.65 \le V_{CC} \le 1.95$	$0.65 \times V_{CC}$		$0.65 \times V_{CC}$			
		$2.30 \le V_{CC} \le 2.70$	1.6		1.6			
		$2.70 \le V_{CC} \le 3.60$	2.0		2.0			
V_{IL}	LOW Level Input Voltage	0.90		$0.35 \times V_{CC}$		$0.35 \times V_{CC}$	V	
		$1.10 \le V_{CC} \le 1.30$		$0.35 \times V_{CC}$		$0.35 \times V_{CC}$		
		$1.40 \le V_{CC} \le 1.60$		$0.35 \times V_{CC}$		$0.35 \times V_{CC}$		
		$1.65 \le V_{CC} \le 1.95$		$0.35 \times V_{CC}$		$0.35 \times V_{CC}$		
		$2.30 \le V_{CC} \le 2.70$		0.7		0.7		
		$2.70 \le V_{CC} \le 3.60$		0.8		0.8		
V_{OH}	HIGH Level Output Voltage	0.90	$V_{CC} - 0.1$		$V_{CC} - 0.1$		V	$I_{OH} = -100$ mA
		$1.10 \le V_{CC} \le 1.30$	$V_{CC} - 0.1$		$V_{CC} - 0.1$			
		$1.40 \le V_{CC} \le 1.60$	$V_{CC} - 0.2$		$V_{CC} - 0.2$			
		$1.65 \le V_{CC} \le 1.95$	$V_{CC} - 0.2$		$V_{CC} - 0.2$			
		$2.30 \le V_{CC} \le 2.70$	$V_{CC} - 0.2$		$V_{CC} - 0.2$			
		$2.70 \le V_{CC} \le 3.60$	$V_{CC} - 0.2$		$V_{CC} - 0.2$			
		$1.10 \le V_{CC} \le 1.30$	$0.75 \times V_{CC}$		$0.75 \times V_{CC}$			$I_{OH} = -2.0$ mA
		$1.40 \le V_{CC} \le 1.60$	$0.75 \times V_{CC}$		$0.75 \times V_{CC}$			$I_{OH} = -4.0$ mA
		$1.65 \le V_{CC} \le 1.95$	1.25		1.25			$I_{OH} = -6.0$ mA
		$2.30 \le V_{CC} \le 2.70$	2.0		2.0			
		$2.30 \le V_{CC} \le 2.70$	1.8		1.8			$I_{OH} = -12.0$ mA
		$2.70 \le V_{CC} \le 3.60$	2.2		2.2			
		$2.30 \le V_{CC} \le 2.70$	1.7		1.7			$I_{OH} = -18.0$ mA
		$2.70 \le V_{CC} \le 3.60$	2.4		2.4			
		$2.70 \le V_{CC} \le 3.60$	2.2		2.2			$I_{OH} = -24.0$ mA
V_{OL}	LOW Level Output Voltage	0.90		0.1		0.1	V	$I_{OL} = 100$ mA
		$1.10 \le V_{CC} \le 1.30$		0.1		0.1		
		$1.40 \le V_{CC} \le 1.60$		0.2		0.2		
		$1.65 \le V_{CC} \le 1.95$		0.2		0.2		
		$2.30 \le V_{CC} \le 2.70$		0.2		0.2		
		$2.70 \le V_{CC} \le 3.60$		0.2		0.2		
		$1.10 \le V_{CC} \le 1.30$		$0.25 \times V_{CC}$		$0.25 \times V_{CC}$		$I_{OL} = 2.0$ mA
		$1.40 \le V_{CC} \le 1.60$		$0.25 \times V_{CC}$		$0.25 \times V_{CC}$		$I_{OL} = 4.0$ mA
		$1.65 \le V_{CC} \le 1.95$		0.3		0.3		$I_{OL} = 6.0$ mA
		$2.30 \le V_{CC} \le 2.70$		0.4		0.4		$I_{OL} = 12.0$ mA
		$2.70 \le V_{CC} \le 3.60$		0.4		0.4		
		$2.30 \le V_{CC} \le 2.70$		0.6		0.6		$I_{OL} = 18.0$ mA
		$2.70 \le V_{CC} \le 3.60$		0.4		0.4		
		$2.70 \le V_{CC} \le 3.60$		0.55		0.55		$I_{OL} = 24.0$ mA
I_{IN}	Input Leakage Current	0.90 to 3.60		±0.1		±0.5	mA	$0 \le V_I \le 3.6V$
I_{OFF}	Power Off Leakage Current	0		0.5		0.5	mA	$0 \le (V_I, V_O) \le 3.6V$
I_{CC}	Quiescent Supply Current	0.90 to 3.60		0.9		0.9	mA	$V_I = V_{CC}$ or GND
		0.90 to 3.60				±0.9		$V_{CC} \le V_I \le 3.6V$

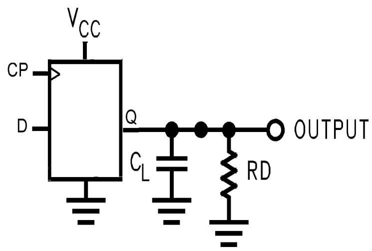
AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$ Min.	Typ.	Max.	$T_A = -40°C$ to $+85°C$ Min.	Max.	Units	Conditions	Figure Number
f_{MAX}	Maximum Clock Frequency	0.90		50				MHz	$C_L = 15$ pF, $R_L = 1$ MΩ	Figure 1, Figure 5
		$1.10 \le V_{CC} \le 1.30$	150			150			$C_L = 15$ pF, $R_L = 2$ kΩ	
		$1.40 \le V_{CC} \le 1.60$	200			200				
		$1.65 \le V_{CC} \le 1.95$	200			200			$C_L = 30$ pF, $R_L = 500Ω$	
		$2.30 \le V_{CC} \le 2.70$	200			200				
		$2.70 \le V_{CC} \le 3.60$	200			200				
t_{PLH}, t_{PHL}	Propagation Delay CK to Q, $\overline{Q}$	0.90		13.0				ns	$C_L = 15$ pF, $R_L = 1$ MΩ	Figure 1, Figure 3
		$1.10 \le V_{CC} \le 1.30$	3.0	6.0	9.9	1.0	14.6		$C_L = 15$ pF, $R_L = 2$ kΩ	
		$1.40 \le V_{CC} \le 1.60$	1.0	3.2	6.0	1.0	7.2			
		$1.65 \le V_{CC} \le 1.95$	1.0	1.9	4.5	1.0	5.3		$C_L = 30$ pF, $R_L = 500$ Ω	
		$2.30 \le V_{CC} \le 2.70$	0.8	1.2	3.0	0.7	3.7			
		$2.70 \le V_{CC} \le 3.60$	0.7	1.0	2.8	0.6	3.2			
t_{PLH}, t_{PHL}	Propagation Delay $\overline{CLR}$, $\overline{PR}$, to Q, $\overline{Q}$	0.90		14.0				ns	$C_L = 15$ pF, $R_L = 1$ MΩ	Figure 1, Figure 3
		$1.10 \le V_{CC} \le 1.30$	3.0	6.5	10.5	1.0	15.1		$C_L = 15$ pF, $R_L = 2$ kΩ	
		$1.40 \le V_{CC} \le 1.60$	1.0	3.2	6.0	1.0	7.2			
		$1.65 \le V_{CC} \le 1.95$	1.0	1.9	4.5	1.0	5.3		$C_L = 30$ pF, $R_L = 500$ Ω	
		$2.30 \le V_{CC} \le 2.70$	0.8	1.2	3.0	0.7	3.7			
		$2.70 \le V_{CC} \le 3.60$	0.7	1.0	2.8	0.6	3.2			
t_S	Setup Time, CK to D	0.90		6.5		6.5		ns	$C_L = 15$ pF, $R_L = 1$ MΩ	Figure 1, Figure 4
		$1.10 \le V_{CC} \le 1.30$	3.5			3.5			$C_L = 15$ pF, $R_L = 2$ kΩ	
		$1.40 \le V_{CC} \le 1.60$	2.0			2.0				
		$1.65 \le V_{CC} \le 1.95$	1.5			1.5			$C_L = 30$ pF, $R_L = 500$ Ω	
		$2.30 \le V_{CC} \le 2.70$	2.0			2.0				
		$2.70 \le V_{CC} \le 3.60$	1.5			1.5				
t_H	Hold Time, CK to D	0.90		0.5		0.5		ns	$C_L = 15$ pF, $R_L = 1$ MΩ	Figure 1, Figure 4
		$1.10 \le V_{CC} \le 1.30$	0.5			0.5			$C_L = 15$ pF, $R_L = 2$ kΩ	
		$1.40 \le V_{CC} \le 1.60$	0.5			0.5				
		$1.65 \le V_{CC} \le 1.95$	0.5			0.5			$C_L = 30$ pF, $R_L = 500$ Ω	
		$2.30 \le V_{CC} \le 2.70$	0.5			0.5				
		$2.70 \le V_{CC} \le 3.60$	0.5			0.5				
t_W	Pulse Width, CK, $\overline{PR}$, $\overline{CLR}$	0.90		7.0		7.0		ns	$C_L = 15$ pF, $R_L = 1$ MΩ	Figure 1, Figure 5
		$1.10 \le V_{CC} \le 1.30$	4.0			4.0			$C_L = 15$ pF, $R_L = 2$ kΩ	
		$1.40 \le V_{CC} \le 1.60$	3.0			3.0				
		$1.65 \le V_{CC} \le 1.95$	3.0			3.0			$C_L = 30$ pF, $R_L = 500Ω$	
		$2.30 \le V_{CC} \le 2.70$	3.0			3.0				
		$2.70 \le V_{CC} \le 3.60$	3.0			3.0				
t_{REC}	Recover Time $\overline{CLR}$, $\overline{PR}$ to CK	0.90		8.0		8.0		ns	$C_L = 15$ pF, $R_L = 1$ MΩ	Figure 1, Figure 4
		$1.10 \le V_{CC} \le 1.30$	4.5			4.5			$C_L = 15$ pF, $R_L = 2$ kΩ	
		$1.40 \le V_{CC} \le 1.60$	3.0			3.0				
		$1.65 \le V_{CC} \le 1.95$	3.0			3.0			$C_L = 30$ pF, $R_L = 500Ω$	
		$2.30 \le V_{CC} \le 2.70$	3.0			3.0				
		$2.70 \le V_{CC} \le 3.60$	3.0			3.0				

Capacitance

Symbol	Parameter	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance	2.0		pF	$V_{CC} = 0V$
C_{OUT}	Output Capacitance	4.5		pF	$V_{CC} = 0V$
C_{PD}	Power Dissipation Capacitance	20.0		pF	$V_I = V_{CC}$ or 0V, f = 10 MHz

AC Loading and Waveforms

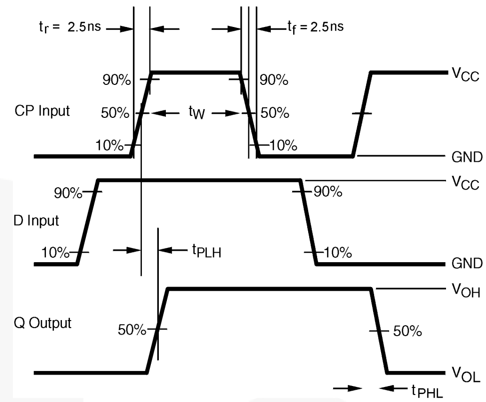


C_L includes load and stray capacitance

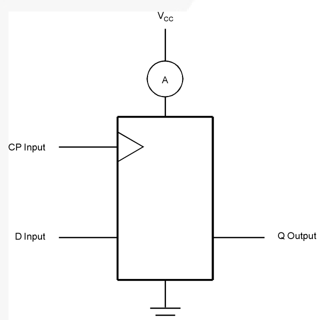
Input PRR = 1.0 MHz; t_w = 500 ns

AC Test Circuit

Test	Switch
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at V_{CC} = 3.3V ± 0.3V V_{CC} x 2 at V_{CC} = < 3.0V
t_{PZH}, t_{PHZ}	GND



AC Waveforms

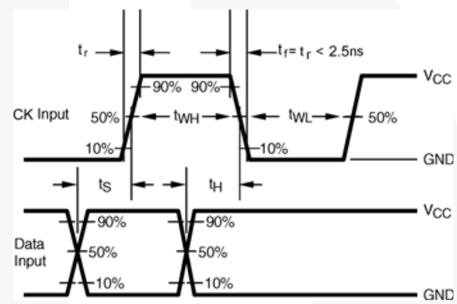


CP Input = AC Waveform; t_r = t_f = 2.5 ns;

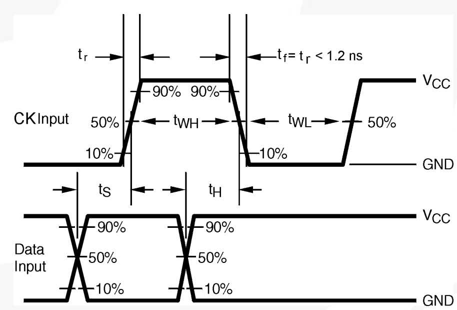
CP Input PRR = 10 MHz; Duty Cycle = 50%

D Input PRR = 5MHz; Duty Cycle = 50%

I_{CCD} Test Circuit



AC Waveforms



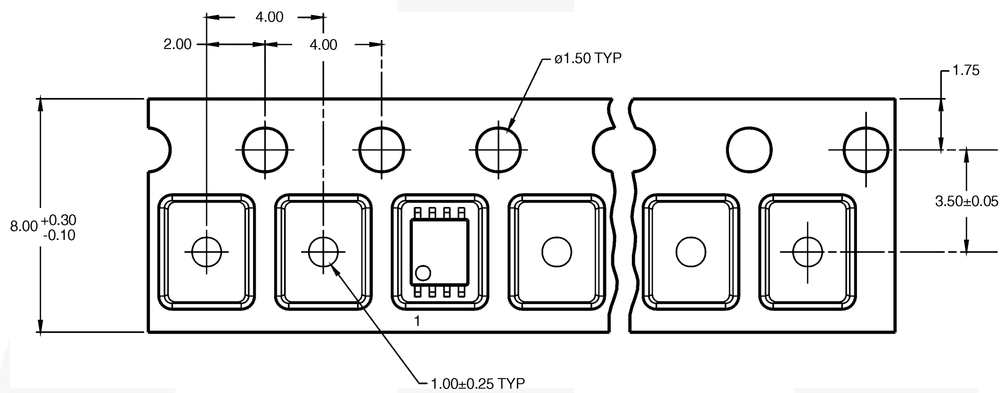
AC Waveforms

Tape and Reel Specification

TAPE FORMAT for US8

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
	Leader (Start End)	125 (typ)	Empty	Sealed
K8X	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

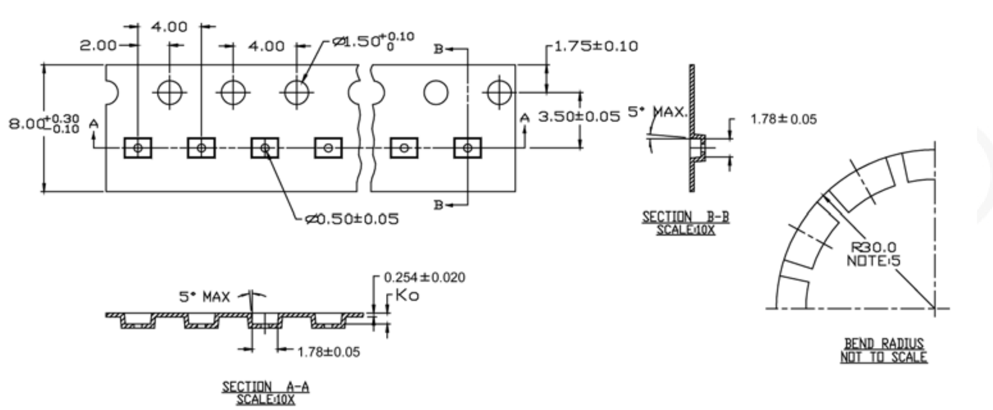
TAPE DIMENSIONS inches (millimeters)



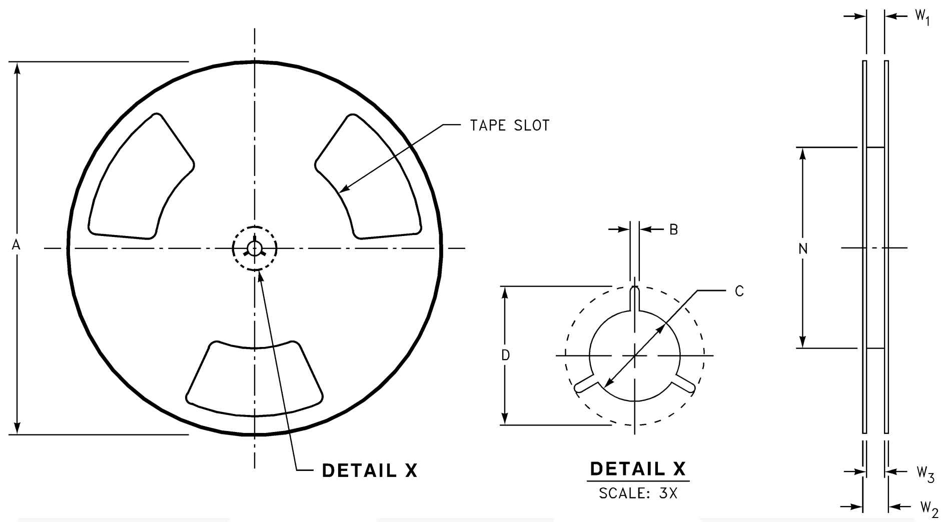
TAPE FORMAT for MicroPak

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
	Leader (Start End)	125 (typ)	Empty	Sealed
L8X	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

TAPE DIMENSIONS inches (millimeters)

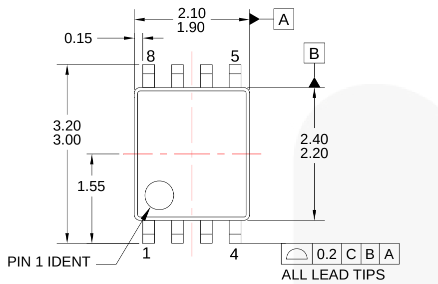


REEL DIMENSIONS inches (millimeters)

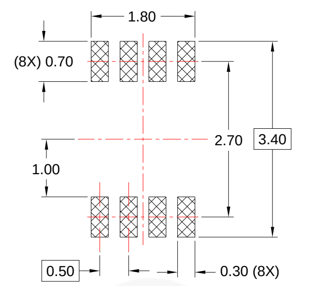


Tape Size	A	B	C	D	N	W1	W2	W3
8 mm	7.0 (177.8)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.331 + 0.059/-0.000 (8.40 + 1.50/-0.00)	0.567 (14.40)	W1 + 0.078/-0.039 (W1 + 2.00/-1.00)

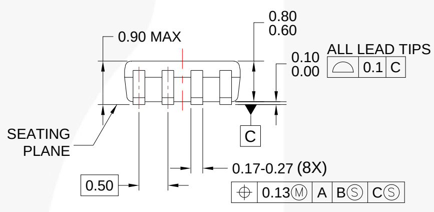
Physical Dimensions



TOP VIEW



RECOMMENDED LAND PATTERN



SIDE VIEW

NOTES:

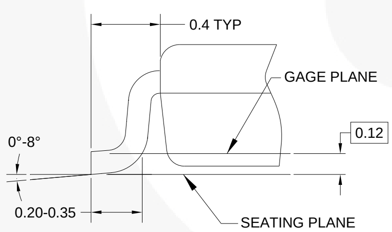
A. CONFORMS TO JEDEC REGISTRATION MO-187

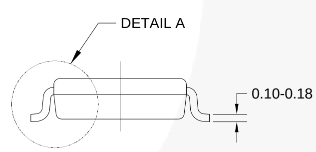
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1994.

E. FILE DRAWING NAME : MKT-MAB08Arev4





DETAIL A

8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide
Package Number MAB08A

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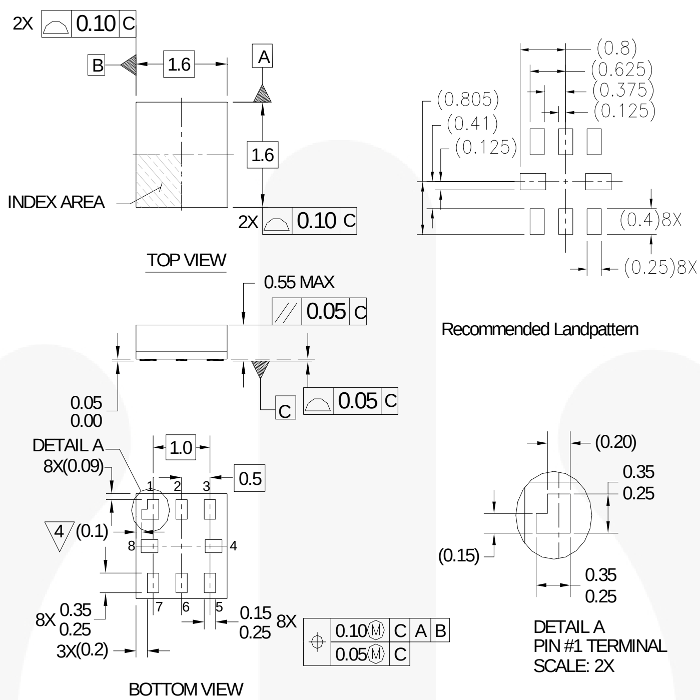
Physical Dimensions



Notes:

1. PACKAGE CONFORMS TO JEDEC MO-255 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y.14M-1994
4. PIN 1 FLAG, END OF PACKAGE OFFSET
5. DRAWING FILE NAME: MKT-MAC08AREV4

MAC08AREV4

Pb-Free 8-Lead MicroPak, 1.6 mm Wide
Package Number MAC08A

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