## Ordering Information

| Part Number | Memory | | Maximum number of I\O's |
|---|---|---|---|
| | Flash (KB) | SRAM (KB) | |
| MKL04Z8VFK4 | 8 | 1 | 22 |
| MKL04Z16VFK4 | 16 | 2 | 22 |
| MKL04Z32VFK4 | 32 | 4 | 22 |
| MKL04Z8VLC4 | 8 | 1 | 28 |
| MKL04Z16VLC4 | 16 | 2 | 28 |
| MKL04Z32VLC4 | 32 | 4 | 28 |
| MKL04Z8VFM4 | 8 | 1 | 28 |
| MKL04Z16VFM4 | 16 | 2 | 28 |
| MKL04Z32VFM4 | 32 | 4 | 28 |
| MKL04Z16VLF4 | 16 | 2 | 41 |
| MKL04Z32VLF4 | 32 | 4 | 41 |

## Related Resources

| Type | Description |
|---|---|
| Selector Guide | The Freescale Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector. |
| Product Brief | The Product Brief contains concise overview/summary information to enable quick evaluation of a device for design suitability. |
| Reference Manual | The Reference Manual contains a comprehensive description of the structure and function (operation) of a device. |
| Data Sheet | The Data Sheet includes electrical characteristics and signal connections. |
| Chip Errata | The chip mask set Errata provides additional or corrective information for a particular device mask set. |
| Package drawing | Package dimensions are provided in package drawings. |

# Table of Contents

# 1 Ratings

## 1.1 Thermal handling ratings

**Table 1. Thermal handling ratings**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $T_{STG}$ | Storage temperature | –55 | 150 | °C | 1 |
| $T_{SDR}$ | Solder temperature, lead-free | — | 260 | °C | 2 |

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 1.2 Moisture handling ratings

**Table 2. Moisture handling ratings**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| MSL | Moisture sensitivity level | — | 3 | — | 1 |

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 1.3 ESD handling ratings

**Table 3. ESD handling ratings**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{HBM}$ | Electrostatic discharge voltage, human body model | –2000 | +2000 | V | 1 |
| $V_{CDM}$ | Electrostatic discharge voltage, charged-device model | –500 | +500 | V | 2 |
| $I_{LAT}$ | Latch-up current at ambient temperature of 105 °C | –100 | +100 | mA | 3 |

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

## 1.4 Voltage and current operating ratings

**Table 4. Voltage and current operating ratings**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$ | Digital supply voltage | –0.3 | 3.8 | V |
| $I_{DD}$ | Digital supply current | — | 120 | mA |
| $V_{IO}$ | IO pin input voltage | –0.3 | $V_{DD}$ + 0.3 | V |
| $I_D$ | Instantaneous maximum current single pin limit (applies to all port pins) | –25 | 25 | mA |
| $V_{DDA}$ | Analog supply voltage | $V_{DD}$ – 0.3 | $V_{DD}$ + 0.3 | V |

# 2 General

## 2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

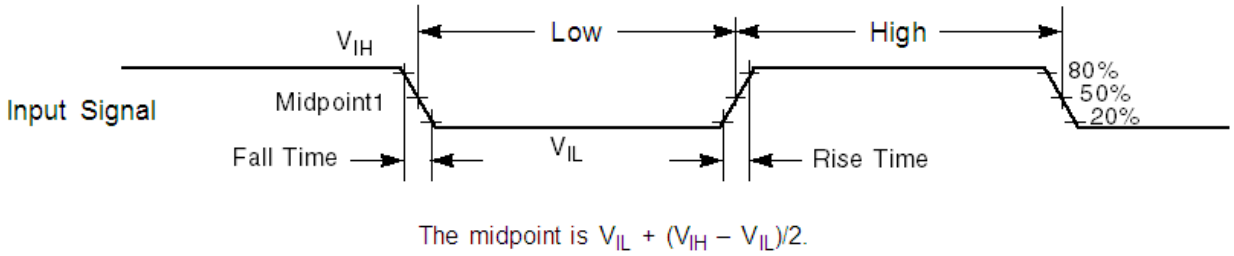



**Figure 1. Input signal measurement reference**

All digital I/O switching characteristics, unless otherwise specified, assume the output pins have the following characteristics.

- $C_L$=30 pF loads
- Slew rate disabled
- Normal drive strength

## 2.2 Nonswitching electrical specifications

## 2.2.1 Voltage and current operating requirements

### Table 5. Voltage and current operating requirements

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 1.71 | 3.6 | V | |
| $V_{DDA}$ | Analog supply voltage | 1.71 | 3.6 | V | — |
| $V_{DD} – V_{DDA}$ | $V_{DD}$-to-$V_{DDA}$ differential voltage | –0.1 | 0.1 | V | — |
| $V_{SS} – V_{SSA}$ | $V_{SS}$-to-$V_{SSA}$ differential voltage | –0.1 | 0.1 | V | — |
| $V_{IH}$ | Input high voltage<br>• 2.7 V ≤ $V_{DD}$ ≤ 3.6 V<br>• 1.7 V ≤ $V_{DD}$ ≤ 2.7 V | <br>0.7 × $V_{DD}$<br>0.75 × $V_{DD}$ | <br>—<br>— | <br>V<br>V | — |
| $V_{IL}$ | Input low voltage<br>• 2.7 V ≤ $V_{DD}$ ≤ 3.6 V<br>• 1.7 V ≤ $V_{DD}$ ≤ 2.7 V | <br>—<br>— | <br>0.35 × $V_{DD}$<br>0.3 × $V_{DD}$ | <br>V<br>V | — |
| $V_{HYS}$ | Input hysteresis | 0.06 × $V_{DD}$ | — | V | — |
| $I_{ICIO}$ | IO pin negative DC injection current—single pin<br>• $V_{IN}$ < $V_{SS}$–0.3V (negative current injection)<br>• $V_{IN}$ < $V_{SS}$–0.3V (positive current injection) | <br>–3<br>— | <br>—<br>+3 | <br>mA | 1 |
| $I_{ICcont}$ | Contiguous pin DC injection current —regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins<br>• Negative current injection<br>• Positive current injection | <br>–25<br>— | <br>—<br>+25 | <br>mA | — |
| $V_{ODPU}$ | Open drain pullup voltage level | $V_{DD}$ | $V_{DD}$ | V | 2 |
| $V_{RAM}$ | $V_{DD}$ voltage required to retain RAM | 1.2 | — | V | — |

1. All IO pins are internally clamped to $V_{SS}$ and $V_{DD}$ through ESD protection diodes. If $V_{IN}$ is greater than $V_{IO\_MIN}$ (=$V_{SS}$-0.3V) and $V_{IN}$ is less than $V_{IO\_MAX}$(=$V_{DD}$+0.3V) is observed, then there is no need to provide current limiting resistors at the pads. If these limits cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as R=($V_{IO\_MIN}$-$V_{IN}$)/|$I_{ICIO}$|. The positive injection current limiting resistor is calculated as R=($V_{IN}$-$V_{IO\_MAX}$)/|$I_{ICIO}$|. Select the larger of these two calculated resistances.
2. Open drain outputs must be pulled to $V_{DD}$.

## 2.2.2 LVD and POR operating requirements

### Table 6. $V_{DD}$ supply LVD and POR operating requirements

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{POR}$ | Falling $V_{DD}$ POR detect voltage | 0.8 | 1.1 | 1.5 | V | — |
| $V_{LVDH}$ | Falling low-voltage detect threshold — high range (LVDV = 01) | 2.48 | 2.56 | 2.64 | V | — |
| | Low-voltage warning thresholds — high range | | | | | 1 |

*Table continues on the next page...*

**Table 6. $V_{DD}$ supply LVD and POR operating requirements (continued)**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{LVW1H}$ | • Level 1 falling (LVWV = 00) | 2.62 | 2.70 | 2.78 | V | |
| $V_{LVW2H}$ | • Level 2 falling (LVWV = 01) | 2.72 | 2.80 | 2.88 | V | |
| $V_{LVW3H}$ | • Level 3 falling (LVWV = 10) | 2.82 | 2.90 | 2.98 | V | |
| $V_{LVW4H}$ | • Level 4 falling (LVWV = 11) | 2.92 | 3.00 | 3.08 | V | |
| $V_{HYSH}$ | Low-voltage inhibit reset/recover hysteresis — high range | — | ±60 | — | mV | — |
| $V_{LVDL}$ | Falling low-voltage detect threshold — low range (LVDV=00) | 1.54 | 1.60 | 1.66 | V | — |
| | Low-voltage warning thresholds — low range | | | | | 1 |
| $V_{LVW1L}$ | • Level 1 falling (LVWV = 00) | 1.74 | 1.80 | 1.86 | V | |
| $V_{LVW2L}$ | • Level 2 falling (LVWV = 01) | 1.84 | 1.90 | 1.96 | V | |
| $V_{LVW3L}$ | • Level 3 falling (LVWV = 10) | 1.94 | 2.00 | 2.06 | V | |
| $V_{LVW4L}$ | • Level 4 falling (LVWV = 11) | 2.04 | 2.10 | 2.16 | V | |
| $V_{HYSL}$ | Low-voltage inhibit reset/recover hysteresis — low range | — | ±40 | — | mV | — |
| $V_{BG}$ | Bandgap voltage reference | 0.97 | 1.00 | 1.03 | V | — |
| $t_{LPO}$ | Internal low power oscillator period — factory trimmed | 900 | 1000 | 1100 | µs | — |

1. Rising thresholds are falling threshold + hysteresis voltage

## 2.2.3 Voltage and current operating behaviors

**Table 7. Voltage and current operating behaviors**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{OH}$ | Output high voltage — Normal drive pad (except $\overline{\text{RESET}}$) | | | | 1, 2 |
| | • 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OH}$ = –5 mA | $V_{DD}$ – 0.5 | — | V | |
| | • 1.71 V ≤ $V_{DD}$ ≤ 2.7 V, $I_{OH}$ = –1.5 mA | $V_{DD}$ – 0.5 | — | V | |
| $V_{OH}$ | Output high voltage — High drive pad (except RESET_b) | | | | 1, 2 |
| | • 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OH}$ = –18 mA | $V_{DD}$ – 0.5 | — | V | |
| | • 1.71 V ≤ $V_{DD}$ ≤ 2.7 V, $I_{OH}$ = –6 mA | $V_{DD}$ – 0.5 | — | V | |
| $I_{OHT}$ | Output high current total for all ports | — | 100 | mA | |
| $V_{OL}$ | Output low voltage — Normal drive pad | | | | 1 |
| | • 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OL}$ = 5 mA | — | 0.5 | V | |
| | • 1.71 V ≤ $V_{DD}$ ≤ 2.7 V, $I_{OL}$ = 1.5 mA | — | 0.5 | V | |

*Table continues on the next page...*

**Table 7. Voltage and current operating behaviors (continued)**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{OL}$ | Output low voltage — High drive pad<br>• 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OL}$ = 18 mA<br>• 1.71 V ≤ $V_{DD}$ ≤ 2.7 V, $I_{OL}$ = 6 mA | <br>—<br>— | <br>0.5<br>0.5 | <br>V<br>V | 1 |
| $I_{OLT}$ | Output low current total for all ports | — | 100 | mA | |
| $I_{IN}$ | Input leakage current (per pin) for full temperature range | — | 1 | µA | 3 |
| $I_{IN}$ | Input leakage current (per pin) at 25 °C | — | 0.025 | µA | 3 |
| $I_{IN}$ | Input leakage current (total all pins) for full temperature range | — | 41 | µA | 3 |
| $I_{OZ}$ | Hi-Z (off-state) leakage current (per pin) | — | 1 | µA | |
| $R_{PU}$ | Internal pullup resistors | 20 | 50 | kΩ | 4 |

1. PTA12, PTA13, PTB0 and PTB1 I/O have both high drive and normal drive capability selected by the associated PTx_PCRn[DSE] control bit. All other GPIOs are normal drive only.
2. The reset pin only contains an active pull down device when configured as the RESET signal or as a GPIO. When configured as a GPIO output, it acts as a pseudo open drain output.
3. Measured at $V_{DD}$ = 3.6 V
4. Measured at $V_{DD}$ supply voltage = $V_{DD}$ min and Vinput = $V_{SS}$

## 2.2.4 Power mode transition operating behaviors

All specifications except $t_{POR}$ and VLLSx→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 48 MHz
- Bus and flash clock = 24 MHz
- FEI clock mode

POR and VLLSx→RUN recovery use FEI clock mode at the default CPU and system frequency of 21 MHz, and a bus and flash clock frequency of 10.5 MHz.

**Table 8. Power mode transition operating behaviors**

| Symbol | Description | Min. | Typ. | Max. | Unit | |
|---|---|---|---|---|---|---|
| $t_{POR}$ | After a POR event, amount of time from the point $V_{DD}$ reaches 1.8 V to execution of the first instruction across the operating temperature range of the chip. | — | — | 300 | µs | 1 |
| | • VLLS0 → RUN | — | 95 | 115 | µs | |
| | • VLLS1 → RUN | | | | | |

*Table continues on the next page...*

**Table 8. Power mode transition operating behaviors (continued)**

| Symbol | Description | Min. | Typ. | Max. | Unit | |
|---|---|---|---|---|---|---|
| | | — | 93 | 115 | µs | |
| | • VLLS3 → RUN | — | 42 | 53 | µs | |
| | • LLS → RUN | — | 4 | 4.6 | µs | |
| | • VLPS → RUN | — | 4 | 4.4 | µs | |
| | • STOP → RUN | — | 4 | 4.4 | µs | |

1. Normal boot (FTFA_FOPT[LPBOOT]=11).

## 2.2.5 Power consumption operating behaviors

The maximum values stated in the following table represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).

**Table 9. Power consumption operating behaviors**

| Symbol | Description | Min. | Typ. | Max.[1] | Unit | Notes |
|---|---|---|---|---|---|---|
| $I_{DDA}$ | Analog supply current | — | — | See note | mA | 2 |
| $I_{DD\_RUNCO}$ | Run mode current in compute operation - 48 MHz core / 24 MHz flash / bus clock disabled, code of while(1) loop executing from flash<br>• at 3.0 V | — | 4.0 | 4.3 | mA | 3 |
| $I_{DD\_RUN}$ | Run mode current - 48 MHz core / 24 MHz bus and flash, all peripheral clocks disabled, code executing from flash<br>• at 3.0 V | — | 4.9 | 5.3 | mA | 3 |
| $I_{DD\_RUN}$ | Run mode current - 48 MHz core / 24 MHz bus and flash, all peripheral clocks enabled, code executing from flash<br>• at 3.0 V<br>• at 25 °C<br>• at 125 °C | —<br>— | 5.7<br>6.0 | 5.8<br>6.2 | mA | 3, 4 |
| $I_{DD\_WAIT}$ | Wait mode current - core disabled / 48 MHz system / 24 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled<br>• at 3.0 V | — | 2.7 | 2.9 | mA | 3 |

*Table continues on the next page...*

## Table 9. Power consumption operating behaviors (continued)

| Symbol | Description | Min. | Typ. | Max.[1] | Unit | Notes |
|---|---|---|---|---|---|---|
| $I_{DD\_WAIT}$ | Wait mode current - core disabled / 24 MHz system / 24 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled<br>• at 3.0 V | — | 2.2 | 2.3 | mA | 3 |
| $I_{DD\_PSTOP2}$ | Stop mode current with partial stop 2 clocking option - core and system disabled / 10.5 MHz bus / flash disabled (flash doze enabled)<br>• at 3.0 V | — | 1.5 | 1.7 | mA | 3 |
| $I_{DD\_VLPRCO}$ | Very-low-power run mode current in compute operation - 4 MHz core / 0.8 MHz flash / bus clock disabled, code executing from flash<br>• at 3.0 V | — | 182 | 253 | µA | 5 |
| $I_{DD\_VLPR}$ | Very low power run mode current - 4 MHz core / 0.8 MHz bus and flash, all peripheral clocks disabled, code executing from flash<br>• at 3.0 V | — | 213 | 284 | µA | 5 |
| $I_{DD\_VLPR}$ | Very low power run mode current - 4 MHz core / 0.8 MHz bus and flash, all peripheral clocks enabled, code executing from flash<br>• at 3.0 V | — | 243 | 313 | µA | 4, 5 |
| $I_{DD\_VLPW}$ | Very low power wait mode current - core disabled / 4 MHz system / 0.8 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled<br>• at 3.0 V | — | 111 | 170 | µA | 5 |
| $I_{DD\_STOP}$ | Stop mode current<br>• at 3.0 V<br>• at 25 °C<br>• at 50 °C<br>• at 70 °C<br>• at 85 °C<br>• at 105 °C | <br>—<br>—<br>—<br>—<br>— | <br>257<br>265<br>278<br>295<br>353 | <br>277<br>285<br>303<br>326<br>412 | µA | |
| $I_{DD\_VLPS}$ | Very-low-power stop mode current<br>• at 3.0 V<br>• at 25 °C<br>• at 50 °C<br>• at 70 °C<br>• at 85 °C<br>• at 105 °C | <br>—<br>—<br>—<br>—<br>— | <br>2.25<br>4.08<br>8.10<br>14.18<br>37.07 | <br>5.76<br>8.27<br>14.52<br>23.78<br>58.58 | µA | |
| $I_{DD\_LLS}$ | Low-leakage stop mode current<br>• at 3.0 V | | | | | |

*Table continues on the next page...*

## Table 9. Power consumption operating behaviors (continued)

| Symbol | Description | Min. | Typ. | Max.[1] | Unit | Notes |
|---|---|---|---|---|---|---|
| | • at 25 °C | — | 1.72 | 2.01 | µA | |
| | • at 50 °C | — | 2.52 | 3.18 | | |
| | • at 70 °C | — | 4.32 | 5.94 | | |
| | • at 85 °C | — | 7.18 | 10.00 | | |
| | • at 105 °C | — | 18.67 | 25.65 | | |
| $I_{DD\_VLLS3}$ | Very-low-leakage stop mode 3 current<br>• at 3.0 V | | | | µA | |
| | • at 25 °C | — | 1.16 | 1.36 | | |
| | • at 50 °C | — | 1.78 | 2.27 | | |
| | • at 70 °C | — | 3.23 | 4.38 | | |
| | • at 85 °C | — | 5.57 | 7.53 | | |
| | • at 105 °C | — | 14.80 | 19.74 | | |
| $I_{DD\_VLLS1}$ | Very-low-leakage stop mode 1 current<br>• at 3.0 V | | | | µA | |
| | • at 25°C | — | 0.64 | 0.81 | | |
| | • at 50°C | — | 1.14 | 1.50 | | |
| | • at 70°C | — | 2.35 | 3.20 | | |
| | • at 85°C | — | 4.37 | 5.80 | | |
| | • at 105°C | — | 12.40 | 16.13 | | |
| $I_{DD\_VLLS0}$ | Very-low-leakage stop mode 0 current (SMC_STOPCTRL[PORPO] = 0)<br>• at 3.0 V | | | | µA | |
| | • at 25 °C | — | 0.38 | 0.54 | | |
| | • at 50 °C | — | 0.88 | 1.23 | | |
| | • at 70 °C | — | 2.10 | 2.95 | | |
| | • at 85 °C | — | 4.14 | 5.59 | | |
| | • at 105 °C | — | 12.00 | 15.73 | | |
| $I_{DD\_VLLS0}$ | Very-low-leakage stop mode 0 current (SMC_STOPCTRL[PORPO] = 1)<br>• at 3.0 V | | | | µA | 6 |
| | • at 25 °C | — | 0.30 | 0.45 | | |
| | • at 50 °C | — | 0.79 | 1.12 | | |
| | • at 70 °C | — | 2.01 | 2.82 | | |
| | • at 85 °C | — | 4.05 | 5.45 | | |
| | • at 105 °C | — | 11.96 | 15.63 | | |

1. Data based on characterization results.

2. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
3. MCG configured for FEI mode.
4. Incremental current consumption from peripheral activity is not included.
5. MCG configured for BLPI mode.
6. No brownout

## Table 10. Low power mode peripheral adders — typical value

| Symbol | Description | Temperature (°C) | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | -40 | 25 | 50 | 70 | 85 | 105 | |
| $I_{IREFSTEN4MHz}$ | 4 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 4 MHz IRC enabled. | 56 | 56 | 56 | 56 | 56 | 56 | µA |
| $I_{IREFSTEN32KHz}$ | 32 kHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 32 kHz IRC enabled. | 52 | 52 | 52 | 52 | 52 | 52 | µA |
| $I_{EREFSTEN4MHz}$ | External 4 MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled. | 206 | 228 | 237 | 245 | 251 | 258 | uA |
| $I_{EREFSTEN32KHz}$ | External 32 kHz crystal clock adder by means of the OSC0_CR[EREFSTEN and EREFSTEN] bits. Measured by entering all modes with the crystal enabled.<br>• VLLS1<br>• VLLS3<br>• LLS<br>• VLPS<br>• STOP | <br>440<br>440<br>490<br>510<br>510 | <br>490<br>490<br>490<br>560<br>560 | <br>540<br>540<br>540<br>560<br>560 | <br>560<br>560<br>560<br>560<br>560 | <br>570<br>570<br>570<br>610<br>610 | <br>580<br>580<br>680<br>680<br>680 | nA |
| $I_{CMP}$ | CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption. | 22 | 22 | 22 | 22 | 22 | 22 | µA |
| $I_{RTC}$ | RTC peripheral adder measured by placing the device in VLLS1 mode with external 32 kHz crystal enabled by means of the RTC_CR[OSCE] bit and the RTC ALARM set for 1 minute. Includes ERCLK32K (32 kHz external crystal) power consumption. | 432 | 357 | 388 | 475 | 532 | 810 | nA |
| $I_{UART}$ | UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption.<br>• MCGIRCLK (4 MHz internal reference clock)<br>• OSCERCLK (4 MHz external crystal) | <br>66<br>214 | <br>66<br>237 | <br>66<br>246 | <br>66<br>254 | <br>66<br>260 | <br>66<br>268 | µA |

*Table continues on the next page...*

**Table 10. Low power mode peripheral adders — typical value (continued)**

| Symbol | Description | Temperature (°C) | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | -40 | 25 | 50 | 70 | 85 | 105 | |
| $I_{TPM}$ | TPM peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source configured for output compare generating 100 Hz clock signal. No load is placed on the I/O generating the clock signal. Includes selected clock source and I/O switching currents.<br>• MCGIRCLK (4 MHz internal reference clock)<br>• OSCERCLK (4 MHz external crystal) | 86<br>235 | 86<br>256 | 86<br>265 | 86<br>274 | 86<br>280 | 86<br>287 | µA |
| $I_{BG}$ | Bandgap adder when BGEN bit is set and device is placed in VLPx, LLS, or VLLSx mode. | 45 | 45 | 45 | 45 | 45 | 45 | µA |
| $I_{ADC}$ | ADC peripheral adder combining the measured values at $V_{DD}$ and $V_{DDA}$ by placing the device in STOP or VLPS mode. ADC is configured for low power mode using the internal clock and continuous conversions. | 366 | 366 | 366 | 366 | 366 | 366 | µA |

### 2.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE for run mode, and BLPE for VLPR mode
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA

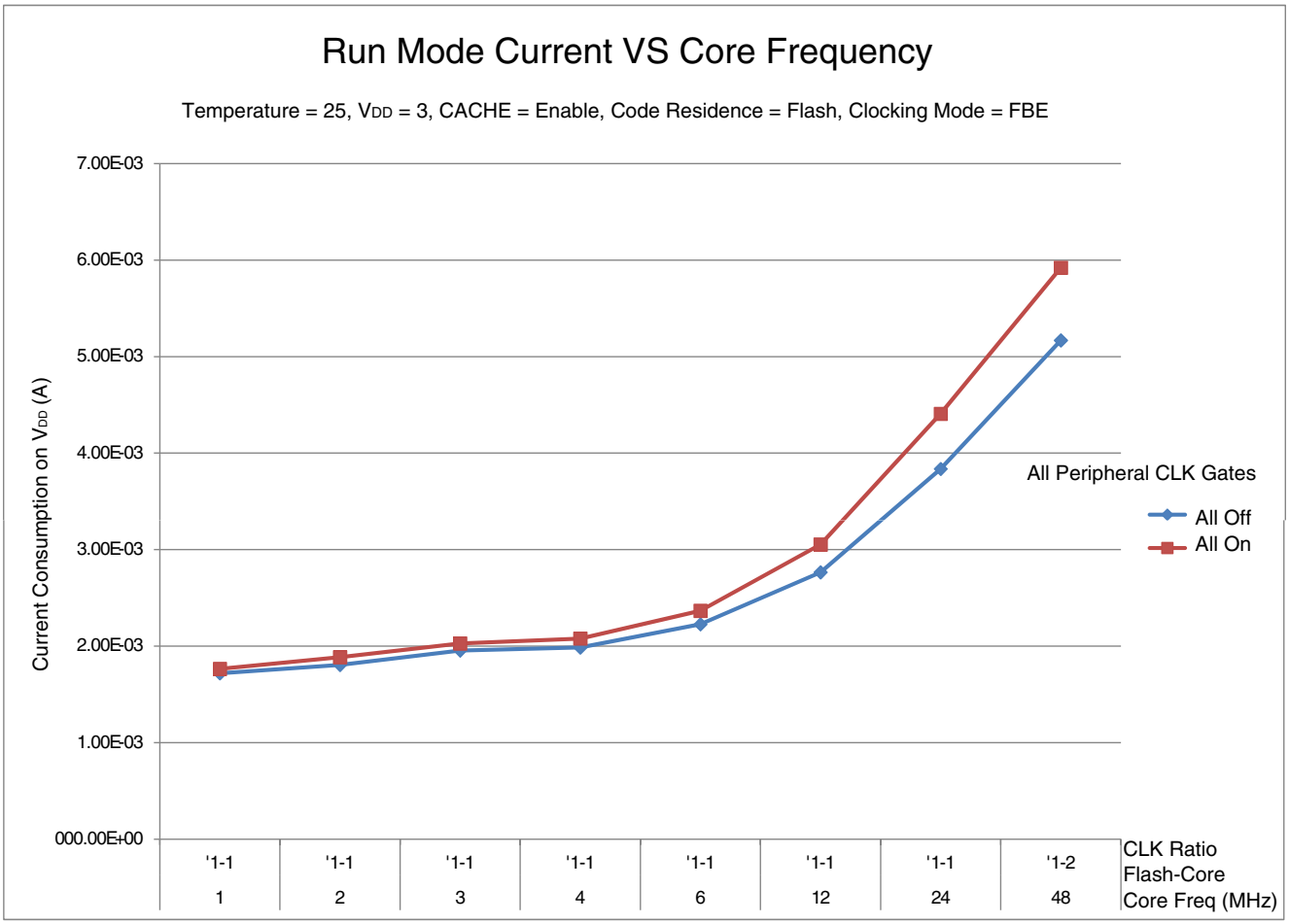



**Figure 2. Run mode supply current vs. core frequency**

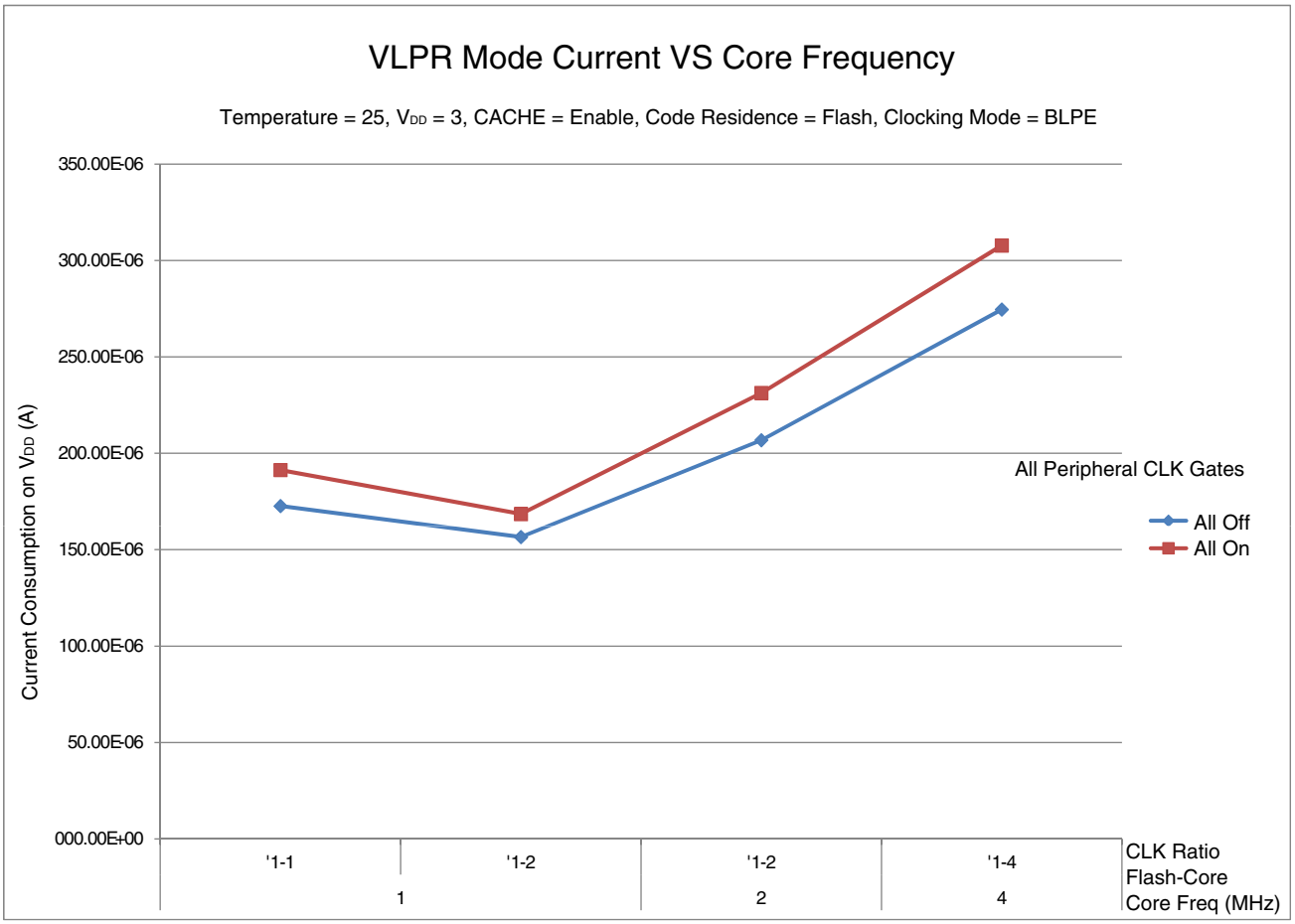



**Figure 3. VLPR mode current vs. core frequency**

## 2.2.6 EMC performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation play a significant role in EMC performance. The system designer must consult the following Freescale applications notes, available on **freescale.com** for advice and guidance specifically targeted at optimizing EMC performance.

- AN2321: Designing for Board Level Electromagnetic Compatibility
- AN1050: Designing for Electromagnetic Compatibility (EMC) with HCMOS Microcontrollers
- AN1263: Designing for Electromagnetic Compatibility with Single-Chip Microcontrollers

- AN2764: Improving the Transient Immunity Performance of Microcontroller-Based Applications
- AN1259: System Design and Layout Techniques for Noise Reduction in MCU-Based Systems

### 2.2.7 Capacitance attributes

**Table 11. Capacitance attributes**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | — | 7 | pF |

## 2.3 Switching specifications

### 2.3.1 Device clock specifications

**Table 12. Device clock specifications**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| Normal run mode | | | | |
| $f_{SYS}$ | System and core clock | — | 48 | MHz |
| $f_{BUS}$ | Bus clock | — | 24 | MHz |
| $f_{FLASH}$ | Flash clock | — | 24 | MHz |
| $f_{LPTMR}$ | LPTMR clock | — | 24 | MHz |
| VLPR and VLPS modes[1] | | | | |
| $f_{SYS}$ | System and core clock | — | 4 | MHz |
| $f_{BUS}$ | Bus clock | — | 1 | MHz |
| $f_{FLASH}$ | Flash clock | — | 1 | MHz |
| $f_{LPTMR}$ | LPTMR clock[2] | — | 24 | MHz |
| $f_{ERCLK}$ | External reference clock | — | 16 | MHz |
| $f_{LPTMR\_ERCLK}$ | LPTMR external reference clock | — | 16 | MHz |
| $f_{osc\_hi\_2}$ | Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x) | — | 16 | MHz |
| $f_{TPM}$ | TPM asynchronous clock | — | 8 | MHz |
| $f_{UART0}$ | UART0 asynchronous clock | — | 8 | MHz |

1. The frequency limitations in VLPR and VLPS modes here override any frequency specification listed in the timing specification for any other module. These same frequency limits apply to VLPS, whether VLPS was entered from RUN or from VLPR.
2. The LPTMR can be clocked at this speed in VLPR or VLPS only when the source is an external pin.

### 2.3.2 General switching specifications

These general-purpose specifications apply to all signals configured for GPIO and UART signals.

**Table 13. General switching specifications**

| Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|
| GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path | 1.5 | — | Bus clock cycles | 1 |
| External RESET and NMI pin interrupt pulse width — Asynchronous path | 100 | — | ns | 2 |
| GPIO pin interrupt pulse width — Asynchronous path | 16 | — | ns | 2 |
| Port rise and fall time | — | 36 | ns | 3 |

1. The greater synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.
3. 75 pF load

## 2.4 Thermal specifications

### 2.4.1 Thermal operating requirements

**Table 14. Thermal operating requirements**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $T_J$ | Die junction temperature | –40 | 125 | °C |
| $T_A$ | Ambient temperature | –40 | 105 | °C |

### 2.4.2 Thermal attributes

**Table 15. Thermal attributes**

| Board type | Symbol | Description | 48 LQFP | 32 LQFP | 32 QFN | 24 QFN | Unit | Notes |
|---|---|---|---|---|---|---|---|---|
| Single-layer (1S) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 82 | 88 | 97 | 110 | °C/W | 1 |
| Four-layer (2s2p) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 58 | 59 | 34 | 42 | °C/W | |

*Table continues on the next page...*

**Table 15. Thermal attributes (continued)**

| Board type | Symbol | Description | 48 LQFP | 32 LQFP | 32 QFN | 24 QFN | Unit | Notes |
|---|---|---|---|---|---|---|---|---|
| Single-layer (1S) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./min. air speed) | 70 | 74 | 81 | 92 | °C/W | |
| Four-layer (2s2p) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./min. air speed) | 52 | 52 | 28 | 36 | °C/W | |
| — | $R_{\theta JB}$ | Thermal resistance, junction to board | 36 | 35 | 13 | 18 | °C/W | 2 |
| — | $R_{\theta JC}$ | Thermal resistance, junction to case | 27 | 26 | 2.3 | 3.7 | °C/W | 3 |
| — | $\Psi_{JT}$ | Thermal characterization parameter, junction to package top outside center (natural convection) | 8 | 8 | 8 | 10 | °C/W | 4 |

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

# 3 Peripheral operating requirements and behaviors

## 3.1 Core modules

### 3.1.1 SWD electricals

**Table 16. SWD full voltage range electricals**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| | Operating voltage | 1.71 | 3.6 | V |
| J1 | SWD_CLK frequency of operation<br>• Serial wire debug | 0 | 25 | MHz |
| J2 | SWD_CLK cycle period | 1/J1 | — | ns |
| J3 | SWD_CLK clock pulse width | | | |

*Table continues on the next page...*

**Table 16. SWD full voltage range electricals (continued)**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| | • Serial wire debug | 20 | — | ns |
| J4 | SWD_CLK rise and fall times | — | 3 | ns |
| J9 | SWD_DIO input data setup time to SWD_CLK rise | 10 | — | ns |
| J10 | SWD_DIO input data hold time after SWD_CLK rise | 0 | — | ns |
| J11 | SWD_CLK high to SWD_DIO data valid | — | 32 | ns |
| J12 | SWD_CLK high to SWD_DIO high-Z | 5 | — | ns |

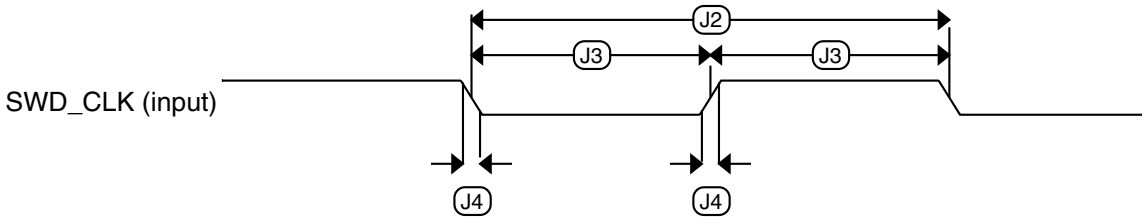



**Figure 4. Serial wire clock input timing**

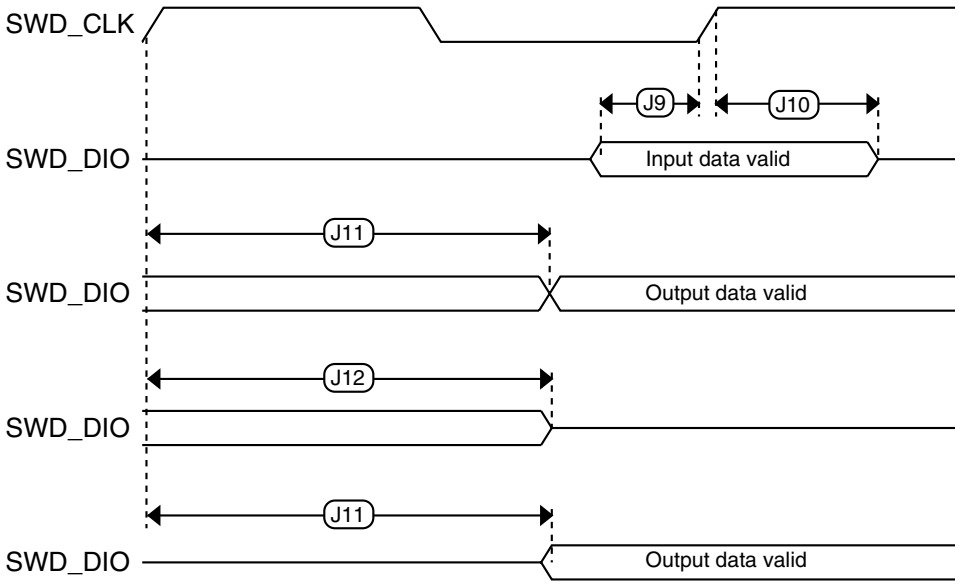



**Figure 5. Serial wire data timing**

## 3.2 System modules

There are no specifications necessary for the device's system modules.

## 3.3 Clock modules

### 3.3.1 MCG specifications

**Table 17. MCG specifications**

| Symbol | Description | | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $f_{ints\_ft}$ | Internal reference frequency (slow clock) — factory trimmed at nominal $V_{DD}$ and 25 °C | | — | 32.768 | — | kHz | |
| $f_{ints\_t}$ | Internal reference frequency (slow clock) — user trimmed | | 31.25 | — | 39.0625 | kHz | |
| $\Delta_{fdco\_res\_t}$ | Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using C3[SCTRIM] and C4[SCFTRIM] | | — | ± 0.3 | ± 0.6 | $\%f_{dco}$ | 1 |
| $\Delta f_{dco\_t}$ | Total deviation of trimmed average DCO output frequency over voltage and temperature | | — | +0.5/-0.7 | ± 3 | $\%f_{dco}$ | 1, 2 |
| $\Delta f_{dco\_t}$ | Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70 °C | | — | ± 0.4 | ± 1.5 | $\%f_{dco}$ | 1, 2 |
| $f_{intf\_ft}$ | Internal reference frequency (fast clock) — factory trimmed at nominal $V_{DD}$ and 25 °C | | — | 4 | — | MHz | |
| $\Delta f_{intf\_ft}$ | Frequency deviation of internal reference clock (fast clock) over temperature and voltage — factory trimmed at nominal $V_{DD}$ and 25 °C | | — | +1/-2 | ± 3 | $\%f_{intf\_ft}$ | 2 |
| $f_{intf\_t}$ | Internal reference frequency (fast clock) — user trimmed at nominal $V_{DD}$ and 25 °C | | 3 | — | 5 | MHz | |
| $f_{loc\_low}$ | Loss of external clock minimum frequency — RANGE = 00 | | (3/5) x $f_{ints\_t}$ | — | — | kHz | |
| $f_{loc\_high}$ | Loss of external clock minimum frequency — | | (16/5) x $f_{ints\_t}$ | — | — | kHz | |
| FLL | | | | | | | |
| $f_{fll\_ref}$ | FLL reference frequency range | | 31.25 | — | 39.0625 | kHz | |
| $f_{dco}$ | DCO output frequency range | Low range (DRS = 00) 640 × $f_{fll\_ref}$ | 20 | 20.97 | 25 | MHz | 3, 4 |
| | | Mid range (DRS = 01) 1280 × $f_{fll\_ref}$ | 40 | 41.94 | 48 | MHz | |
| $f_{dco\_t\_DMX32}$ | DCO output frequency | Low range (DRS = 00) 732 × $f_{fll\_ref}$ | — | 23.99 | — | MHz | 5, 6 |
| | | Mid range (DRS = 01) | — | 47.97 | — | MHz | |

*Table continues on the next page...*

**Table 17. MCG specifications (continued)**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| | 1464 × $f_{fll\_ref}$ | | | | | |
| $J_{cyc\_fll}$ | FLL period jitter<br>• $f_{VCO}$ = 48 MHz | — | 180 | — | ps | 7 |
| $t_{fll\_acquire}$ | FLL target frequency acquisition time | — | — | 1 | ms | 8 |

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. The deviation is relative to the factory trimmed frequency at nominal $V_{DD}$ and 25 °C, $f_{ints\_ft}$.
3. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32 = 0.
4. The resulting system clock frequencies must not exceed their maximum specified values. The DCO frequency deviation ($\Delta f_{dco\_t}$) over voltage and temperature must be considered.
5. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32 = 1.
6. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
7. This specification is based on standard deviation (RMS) of period or frequency.
8. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

## 3.3.2 Oscillator electrical specifications

### 3.3.2.1 Oscillator DC electrical specifications

**Table 18. Oscillator DC electrical specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 1.71 | — | 3.6 | V | |
| $I_{DDOSC}$ | Supply current — low-power mode (HGO=0) | | | | | 1 |
| | • 32 kHz | — | 500 | — | nA | |
| | • 4 MHz | — | 200 | — | µA | |
| | • 8 MHz (RANGE=01) | — | 300 | — | µA | |
| | • 16 MHz | — | 950 | — | µA | |
| | • 24 MHz | — | 1.2 | — | mA | |
| | • 32 MHz | — | 1.5 | — | mA | |
| $I_{DDOSC}$ | Supply current — high gain mode (HGO=1) | | | | | 1 |
| | • 32 kHz | — | 25 | — | µA | |
| | • 4 MHz | — | 400 | — | µA | |
| | • 8 MHz (RANGE=01) | — | 500 | — | µA | |
| | • 16 MHz | — | 2.5 | — | mA | |
| | | — | 3 | — | mA | |
| | | — | 4 | — | mA | |

*Table continues on the next page...*

## Table 18. Oscillator DC electrical specifications (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| | • 24 MHz<br>• 32 MHz | | | | | |
| $C_x$ | EXTAL load capacitance | — | — | — | | 2, 3 |
| $C_y$ | XTAL load capacitance | — | — | — | | 2, 3 |
| $R_F$ | Feedback resistor — low-frequency, low-power mode (HGO=0) | — | — | — | MΩ | 2, 4 |
| | Feedback resistor — low-frequency, high-gain mode (HGO=1) | — | 10 | — | MΩ | |
| | Feedback resistor — high-frequency, low-power mode (HGO=0) | — | — | — | MΩ | |
| | Feedback resistor — high-frequency, high-gain mode (HGO=1) | — | 1 | — | MΩ | |
| $R_S$ | Series resistor — low-frequency, low-power mode (HGO=0) | — | — | — | kΩ | |
| | Series resistor — low-frequency, high-gain mode (HGO=1) | — | 200 | — | kΩ | |
| | Series resistor — high-frequency, low-power mode (HGO=0) | — | — | — | kΩ | |
| | Series resistor — high-frequency, high-gain mode (HGO=1) | — | 0 | — | kΩ | |
| $V_{pp}$[5] | Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0) | — | 0.6 | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1) | — | $V_{DD}$ | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0) | — | 0.6 | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1) | — | $V_{DD}$ | — | V | |

1. $V_{DD}$=3.3 V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. $C_x$,$C_y$ can be provided by using the integrated capacitors when the low frequency oscillator (RANGE = 00) is used. For all other cases external capacitors must be used.
4. When low power mode is selected, $R_F$ is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

#### 3.3.2.2 Oscillator frequency specifications

**Table 19. Oscillator frequency specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $f_{osc\_lo}$ | Oscillator crystal or resonator frequency — low-frequency mode (MCG_C2[RANGE]=00) | 32 | — | 40 | kHz | |
| $f_{osc\_hi\_1}$ | Oscillator crystal or resonator frequency — high-frequency mode (low range) (MCG_C2[RANGE]=01) | 3 | — | 8 | MHz | |
| $f_{osc\_hi\_2}$ | Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x) | 8 | — | 32 | MHz | |
| $f_{ec\_extal}$ | Input clock frequency (external clock mode) | — | — | 48 | MHz | 1, 2 |
| $t_{dc\_extal}$ | Input clock duty cycle (external clock mode) | 40 | 50 | 60 | % | |
| $t_{cst}$ | Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0) | — | | — | ms | 3, 4 |
| | Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1) | — | | — | ms | |
| | Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0) | — | 0.6 | — | ms | |
| | Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1) | — | 1 | — | ms | |

1. Other frequency limits may apply when external clock is being used as a reference for the FLL
2. When transitioning from FEI or FBI to FBE mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
3. Proper PC board layout procedures must be followed to achieve specifications.
4. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

## 3.4 Memories and memory interfaces

### 3.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

#### 3.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

**Table 20. NVM program/erase timing specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $t_{hvpgm4}$ | Longword Program high-voltage time | — | 7.5 | 18 | µs | |
| $t_{hversscr}$ | Sector Erase high-voltage time | — | 13 | 113 | ms | 1 |
| $t_{hversall}$ | Erase All high-voltage time | — | 52 | 452 | ms | 1 |

1. Maximum time based on expectations at cycling end-of-life.

### 3.4.1.2 Flash timing specifications — commands

**Table 21. Flash command timing specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $t_{rd1sec1k}$ | Read 1s Section execution time (flash sector) | — | — | 60 | µs | 1 |
| $t_{pgmchk}$ | Program Check execution time | — | — | 45 | µs | 1 |
| $t_{rdrsrc}$ | Read Resource execution time | — | — | 30 | µs | 1 |
| $t_{pgm4}$ | Program Longword execution time | — | 65 | 145 | µs | |
| $t_{ersscr}$ | Erase Flash Sector execution time | — | 14 | 114 | ms | 2 |
| $t_{rd1all}$ | Read 1s All Blocks execution time | — | — | 0.5 | ms | |
| $t_{rdonce}$ | Read Once execution time | — | — | 25 | µs | 1 |
| $t_{pgmonce}$ | Program Once execution time | — | 65 | — | µs | |
| $t_{ersall}$ | Erase All Blocks execution time | — | 61 | 500 | ms | 2 |
| $t_{vfykey}$ | Verify Backdoor Access Key execution time | — | — | 30 | µs | 1 |

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

### 3.4.1.3 Flash high voltage current behaviors

**Table 22. Flash high voltage current behaviors**

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $I_{DD\_PGM}$ | Average current adder during high voltage flash programming operation | — | 2.5 | 6.0 | mA |
| $I_{DD\_ERS}$ | Average current adder during high voltage flash erase operation | — | 1.5 | 4.0 | mA |

### 3.4.1.4 Reliability specifications

**Table 23. NVM reliability specifications**

| Symbol | Description | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| Program Flash | | | | | | |

*Table continues on the next page...*

**Table 23. NVM reliability specifications (continued)**

| Symbol | Description | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $t_{nvmretp10k}$ | Data retention after up to 10 K cycles | 5 | 50 | — | years | |
| $t_{nvmretp1k}$ | Data retention after up to 1 K cycles | 20 | 100 | — | years | |
| $n_{nvmcycp}$ | Cycling endurance | 10 K | 50 K | — | cycles | 2 |

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at -40 °C ≤ $T_j$ ≤ 125 °C.

## 3.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

## 3.6 Analog

### 3.6.1 ADC electrical specifications

All ADC channels meet the 12-bit single-ended accuracy specifications.

#### 3.6.1.1 12-bit ADC operating conditions

**Table 24. 12-bit ADC operating conditions**

| Symbol | Description | Conditions | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $V_{DDA}$ | Supply voltage | Absolute | 1.71 | — | 3.6 | V | |
| $\Delta V_{DDA}$ | Supply voltage | Delta to $V_{DD}$ ($V_{DD}$ – $V_{DDA}$) | -100 | 0 | +100 | mV | 2 |
| $\Delta V_{SSA}$ | Ground voltage | Delta to $V_{SS}$ ($V_{SS}$ – $V_{SSA}$) | -100 | 0 | +100 | mV | 2 |
| $V_{REFH}$ | ADC reference voltage high | | 1.13 | $V_{DDA}$ | $V_{DDA}$ | V | 3 |
| $V_{REFL}$ | ADC reference voltage low | | $V_{SSA}$ | $V_{SSA}$ | $V_{SSA}$ | V | 3 |
| $V_{ADIN}$ | Input voltage | | $V_{REFL}$ | — | $V_{REFH}$ | V | |
| $C_{ADIN}$ | Input capacitance | • 8-bit / 10-bit / 12-bit modes | — | 4 | 5 | pF | |
| $R_{ADIN}$ | Input series resistance | | — | 2 | 5 | kΩ | |

*Table continues on the next page...*

## Table 24. 12-bit ADC operating conditions (continued)

| Symbol | Description | Conditions | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $R_{AS}$ | Analog source resistance (external) | 12-bit modes<br>$f_{ADCK}$ < 4 MHz | — | — | 5 | kΩ | 4 |
| $f_{ADCK}$ | ADC conversion clock frequency | ≤ 12-bit mode | 1.0 | — | 18.0 | MHz | 5 |
| $C_{rate}$ | ADC conversion rate | ≤ 12-bit modes<br>No ADC hardware averaging<br>Continuous conversions enabled, subsequent conversion time | 20.000 | — | 818.330 | Ksps | 6 |

1. Typical values assume $V_{DDA}$ = 3.0 V, Temp = 25 °C, $f_{ADCK}$ = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. For packages without dedicated VREFH and VREFL pins, $V_{REFH}$ is internally tied to $V_{DDA}$, and $V_{REFL}$ is internally tied to $V_{SSA}$.
4. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8 Ω analog source resistance. The $R_{AS}$/$C_{AS}$ time constant should be kept to < 1 ns.
5. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
6. For guidelines and examples of conversion rate calculation, download the ADC calculator tool.

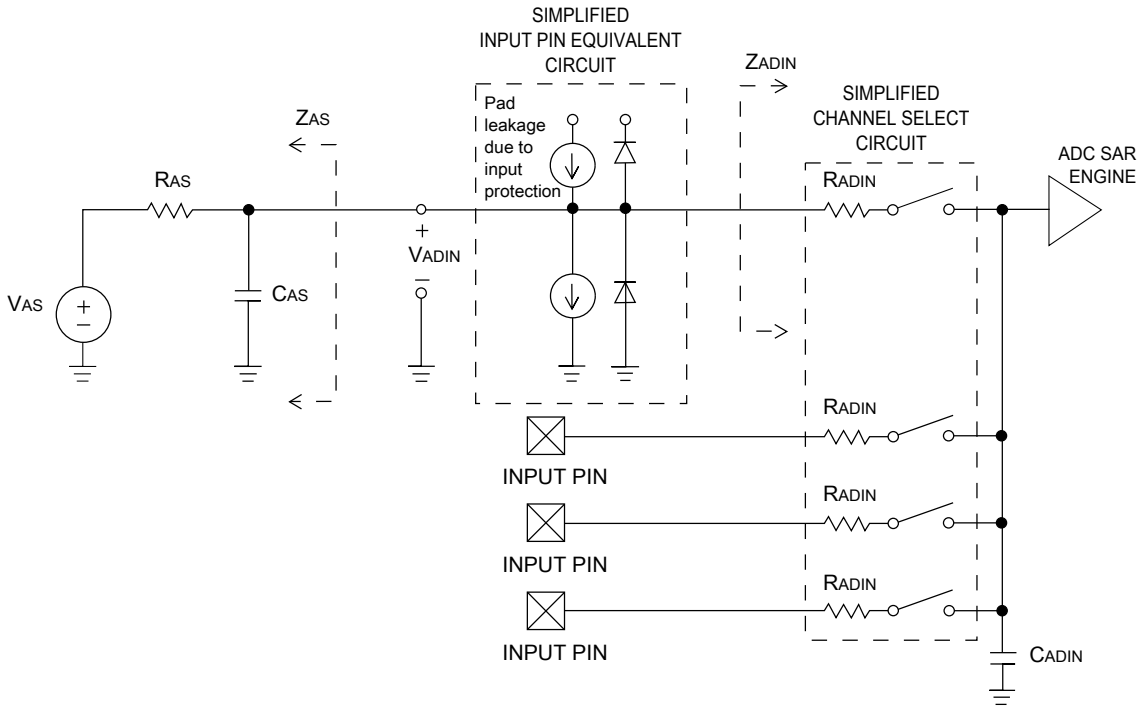



**Figure 6. ADC input impedance equivalency diagram**

### 3.6.1.2 12-bit ADC electrical characteristics

**Table 25. 12-bit ADC characteristics ($V_{REFH}$ = $V_{DDA}$, $V_{REFL}$ = $V_{SSA}$)**

| Symbol | Description | Conditions[1] | Min. | Typ.[2] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $I_{DDA\_ADC}$ | Supply current | | 0.215 | — | 1.7 | mA | 3 |
| $f_{ADACK}$ | ADC asynchronous clock source | • ADLPC = 1, ADHSC = 0<br>• ADLPC = 1, ADHSC = 1<br>• ADLPC = 0, ADHSC = 0<br>• ADLPC = 0, ADHSC = 1 | 1.2<br>2.4<br>3.0<br>4.4 | 2.4<br>4.0<br>5.2<br>6.2 | 3.9<br>6.1<br>7.3<br>9.5 | MHz<br>MHz<br>MHz<br>MHz | $t_{ADACK}$ = 1/ $f_{ADACK}$ |
| | Sample Time | See Reference Manual chapter for sample times | | | | | |
| TUE | Total unadjusted error | • 12-bit modes<br>• <12-bit modes | —<br>— | ±4<br>±1.4 | ±6.8<br>±2.1 | LSB[4] | 5 |
| DNL | Differential non-linearity | • 12-bit modes<br>• <12-bit modes | —<br>— | ±0.7<br>±0.2 | –1.1 to +1.9<br>–0.3 to 0.5 | LSB[4] | 5 |
| INL | Integral non-linearity | • 12-bit modes<br>• <12-bit modes | —<br>— | ±1.0<br>±0.5 | –2.7 to +1.9<br>–0.7 to +0.5 | LSB[4] | 5 |
| $E_{FS}$ | Full-scale error | • 12-bit modes<br>• <12-bit modes | —<br>— | –4<br>–1.4 | –5.4<br>–1.8 | LSB[4] | $V_{ADIN}$ = $V_{DDA}$[5] |
| $E_Q$ | Quantization error | • 12-bit modes | — | — | ±0.5 | LSB[4] | |
| $E_{IL}$ | Input leakage error | | $I_{In} \times R_{AS}$ | | | mV | $I_{In}$ = leakage current (refer to the MCU's voltage and current operating ratings) |
| | Temp sensor slope | Across the full temperature range of the device | 1.55 | 1.62 | 1.69 | mV/°C | 6 |
| $V_{TEMP25}$ | Temp sensor voltage | 25 °C | 706 | 716 | 726 | mV | 6 |

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH}$ = $V_{DDA}$
2. Typical values assume $V_{DDA}$ = 3.0 V, Temp = 25 °C, $f_{ADCK}$ = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
4. 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. ADC conversion clock < 3 MHz

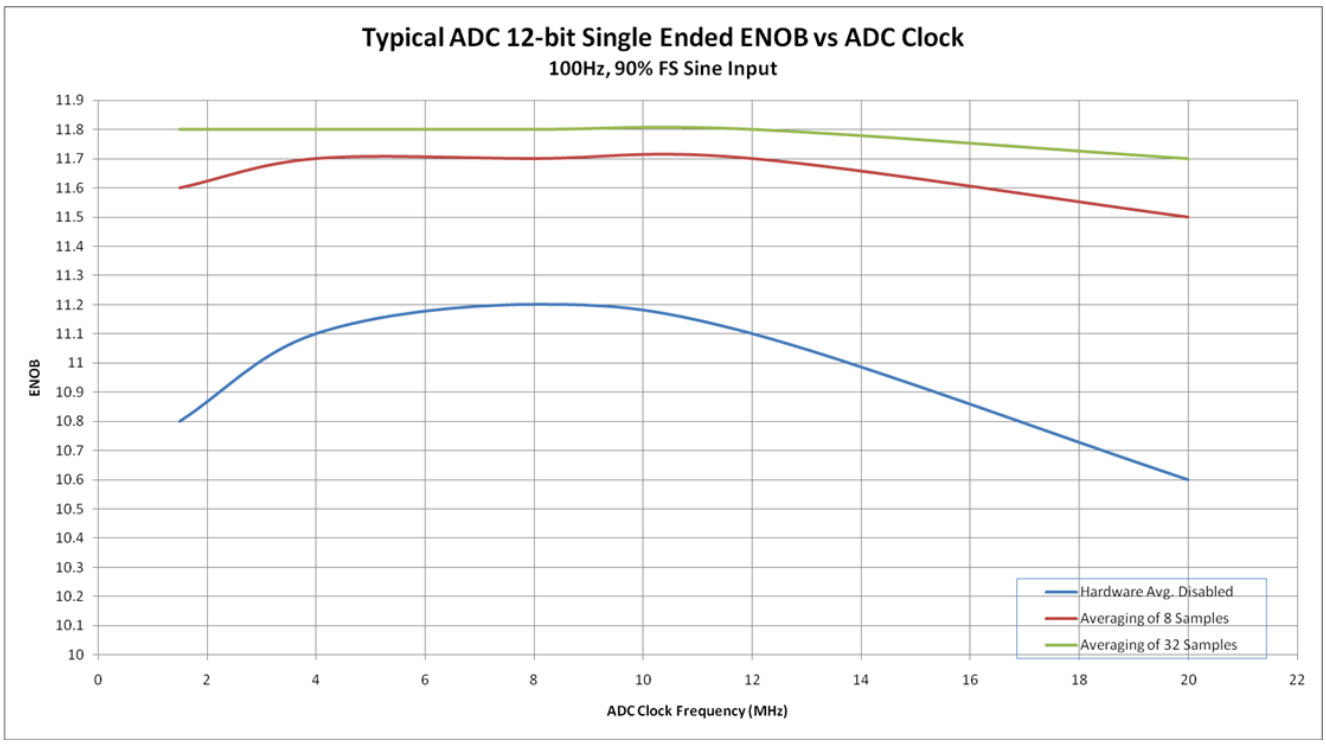



**Figure 7. Typical ENOB vs. ADC_CLK for 12-bit single-ended mode**

## 3.6.2 CMP and 6-bit DAC electrical specifications

**Table 26. Comparator and 6-bit DAC electrical specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 1.71 | — | 3.6 | V |
| $I_{DDHS}$ | Supply current, high-speed mode (EN = 1, PMODE = 1) | — | — | 200 | µA |
| $I_{DDLS}$ | Supply current, low-speed mode (EN = 1, PMODE = 0) | — | — | 20 | µA |
| $V_{AIN}$ | Analog input voltage | $V_{SS}$ | — | $V_{DD}$ | V |
| $V_{AIO}$ | Analog input offset voltage | — | — | 20 | mV |
| $V_H$ | Analog comparator hysteresis[1] | | | | |
| | • CR0[HYSTCTR] = 00 | — | 5 | — | mV |
| | • CR0[HYSTCTR] = 01 | — | 10 | — | mV |

*Table continues on the next page...*

**Table 26. Comparator and 6-bit DAC electrical specifications (continued)**

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| | • CR0[HYSTCTR] = 10 | — | 20 | — | mV |
| | • CR0[HYSTCTR] = 11 | — | 30 | — | mV |
| $V_{CMPOh}$ | Output high | $V_{DD}$ – 0.5 | — | — | V |
| $V_{CMPOl}$ | Output low | — | — | 0.5 | V |
| $t_{DHS}$ | Propagation delay, high-speed mode (EN = 1, PMODE = 1) | 20 | 50 | 200 | ns |
| $t_{DLS}$ | Propagation delay, low-speed mode (EN = 1, PMODE = 0) | 80 | 250 | 600 | ns |
| | Analog comparator initialization delay[2] | — | — | 40 | µs |
| $I_{DAC6b}$ | 6-bit DAC current adder (enabled) | — | 7 | — | µA |
| INL | 6-bit DAC integral non-linearity | –0.5 | — | 0.5 | LSB[3] |
| DNL | 6-bit DAC differential non-linearity | –0.3 | — | 0.3 | LSB |

1. Typical hysteresis is measured with input voltage range limited to 0.7 to $V_{DD}$ – 0.7 V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}$/64

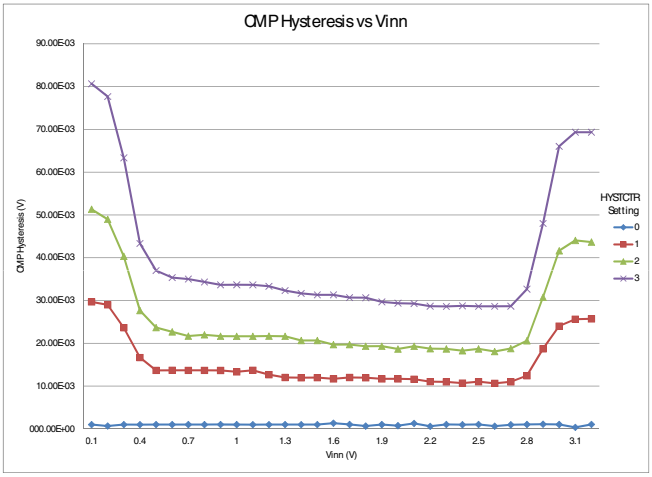



**Figure 8. Typical hysteresis vs. Vin level ($V_{DD}$ = 3.3 V, PMODE = 0)**

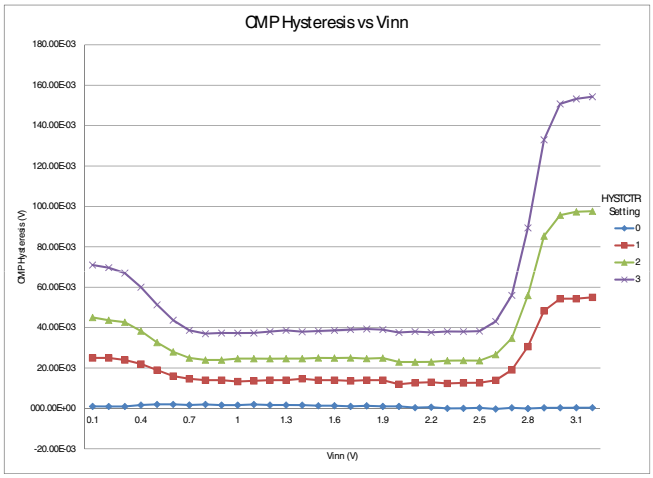



**Figure 9. Typical hysteresis vs. Vin level ($V_{DD}$ = 3.3 V, PMODE = 1)**

## 3.7 Timers

See General switching specifications.

## 3.8 Communication interfaces

### 3.8.1 SPI switching specifications

The Serial Peripheral Interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. See the SPI chapter of the chip's Reference Manual for information about the modified transfer formats used for communicating with slower peripheral devices.

All timing is shown with respect to 20% $V_{DD}$ and 80% $V_{DD}$ thresholds, unless noted, as well as input signal transitions of 3 ns and a 30 pF maximum load on all SPI pins.

**Table 27. SPI master mode timing on slew rate disabled pads**

| Num. | Symbol | Description | Min. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| 1 | $f_{op}$ | Frequency of operation | $f_{periph}/2048$ | $f_{periph}/2$ | Hz | 1 |
| 2 | $t_{SPSCK}$ | SPSCK period | 2 x $t_{periph}$ | 2048 x $t_{periph}$ | ns | 2 |
| 3 | $t_{Lead}$ | Enable lead time | 1/2 | — | $t_{SPSCK}$ | — |
| 4 | $t_{Lag}$ | Enable lag time | 1/2 | — | $t_{SPSCK}$ | — |

*Table continues on the next page...*

## Table 27. SPI master mode timing on slew rate disabled pads (continued)

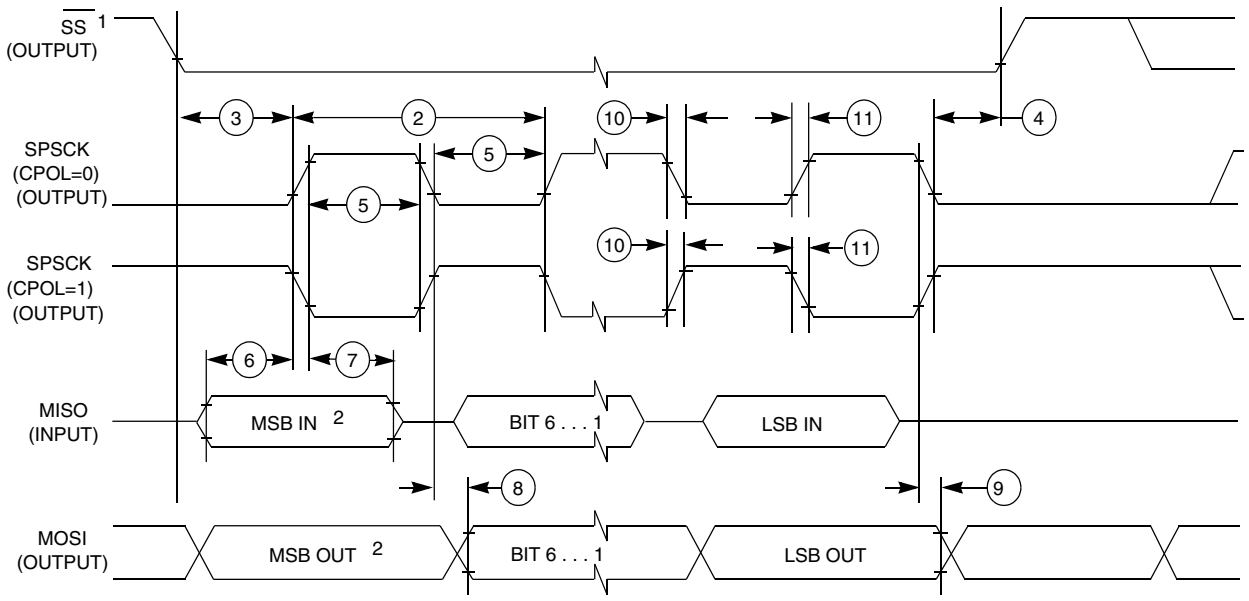
| Num. | Symbol | Description | Min. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| 5 | $t_{WSPSCK}$ | Clock (SPSCK) high or low time | $t_{periph} - 30$ | 1024 x $t_{periph}$ | ns | — |
| 6 | $t_{SU}$ | Data setup time (inputs) | 16 | — | ns | — |
| 7 | $t_{HI}$ | Data hold time (inputs) | 0 | — | ns | — |
| 8 | $t_v$ | Data valid (after SPSCK edge) | — | 10 | ns | — |
| 9 | $t_{HO}$ | Data hold time (outputs) | 0 | — | ns | — |
| 10 | $t_{RI}$ | Rise time input | — | $t_{periph} - 25$ | ns | — |
| | $t_{FI}$ | Fall time input | | | | |
| 11 | $t_{RO}$ | Rise time output | — | 25 | ns | — |
| | $t_{FO}$ | Fall time output | | | | |

1. For SPI0, $f_{periph}$ is the bus clock ($f_{BUS}$).
2. $t_{periph} = 1/f_{periph}$

## Table 28. SPI master mode timing on slew rate enabled pads

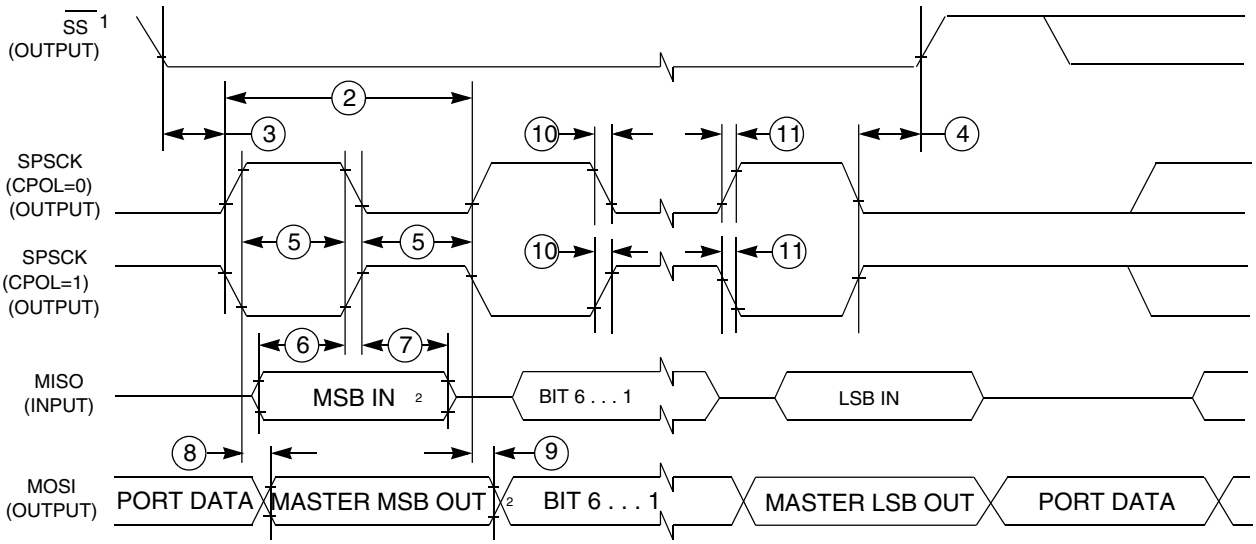
| Num. | Symbol | Description | Min. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| 1 | $f_{op}$ | Frequency of operation | $f_{periph}/2048$ | $f_{periph}/2$ | Hz | 1 |
| 2 | $t_{SPSCK}$ | SPSCK period | 2 x $t_{periph}$ | 2048 x $t_{periph}$ | ns | 2 |
| 3 | $t_{Lead}$ | Enable lead time | 1/2 | — | $t_{SPSCK}$ | — |
| 4 | $t_{Lag}$ | Enable lag time | 1/2 | — | $t_{SPSCK}$ | — |
| 5 | $t_{WSPSCK}$ | Clock (SPSCK) high or low time | $t_{periph} - 30$ | 1024 x $t_{periph}$ | ns | — |
| 6 | $t_{SU}$ | Data setup time (inputs) | 96 | — | ns | — |
| 7 | $t_{HI}$ | Data hold time (inputs) | 0 | — | ns | — |
| 8 | $t_v$ | Data valid (after SPSCK edge) | — | 52 | ns | — |
| 9 | $t_{HO}$ | Data hold time (outputs) | 0 | — | ns | — |
| 10 | $t_{RI}$ | Rise time input | — | $t_{periph} - 25$ | ns | — |
| | $t_{FI}$ | Fall time input | | | | |
| 11 | $t_{RO}$ | Rise time output | — | 36 | ns | — |
| | $t_{FO}$ | Fall time output | | | | |

1. For SPI0, $f_{periph}$ is the bus clock ($f_{BUS}$).
2. $t_{periph} = 1/f_{periph}$




1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

**Figure 10. SPI master mode timing (CPHA = 0)**




1.If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

**Figure 11. SPI master mode timing (CPHA = 1)**

## Table 29. SPI slave mode timing on slew rate disabled pads

| Num. | Symbol | Description | Min. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| 1 | $f_{op}$ | Frequency of operation | 0 | $f_{periph}/4$ | Hz | 1 |
| 2 | $t_{SPSCK}$ | SPSCK period | 4 x $t_{periph}$ | — | ns | 2 |
| 3 | $t_{Lead}$ | Enable lead time | 1 | — | $t_{periph}$ | — |

*Table continues on the next page...*

## Table 29. SPI slave mode timing on slew rate disabled pads (continued)

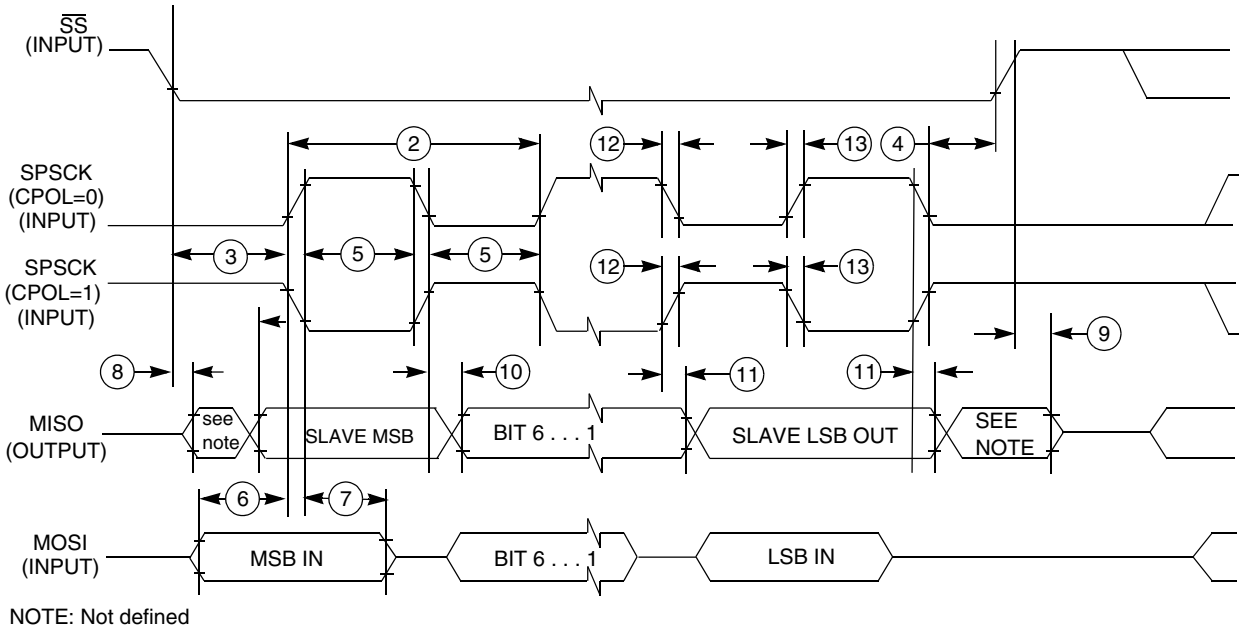
| Num. | Symbol | Description | Min. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| 4 | $t_{Lag}$ | Enable lag time | 1 | — | $t_{periph}$ | — |
| 5 | $t_{WSPSCK}$ | Clock (SPSCK) high or low time | $t_{periph} - 30$ | — | ns | — |
| 6 | $t_{SU}$ | Data setup time (inputs) | 2 | — | ns | — |
| 7 | $t_{HI}$ | Data hold time (inputs) | 7 | — | ns | — |
| 8 | $t_a$ | Slave access time | — | $t_{periph}$ | ns | 3 |
| 9 | $t_{dis}$ | Slave MISO disable time | — | $t_{periph}$ | ns | 4 |
| 10 | $t_v$ | Data valid (after SPSCK edge) | — | 22 | ns | — |
| 11 | $t_{HO}$ | Data hold time (outputs) | 0 | — | ns | — |
| 12 | $t_{RI}$ | Rise time input | — | $t_{periph} - 25$ | ns | — |
| | $t_{FI}$ | Fall time input | | | | |
| 13 | $t_{RO}$ | Rise time output | — | 25 | ns | — |
| | $t_{FO}$ | Fall time output | | | | |

1. For SPI0, $f_{periph}$ is the bus clock ($f_{BUS}$).
2. $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state

## Table 30. SPI slave mode timing on slew rate enabled pads

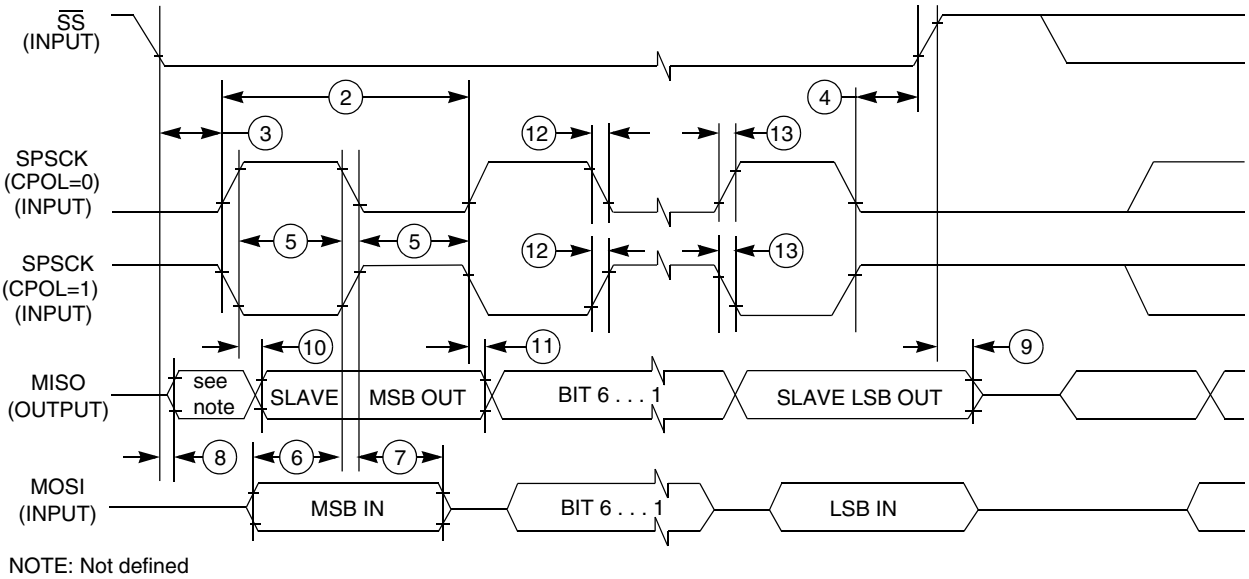
| Num. | Symbol | Description | Min. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| 1 | $f_{op}$ | Frequency of operation | 0 | $f_{periph}/4$ | Hz | 1 |
| 2 | $t_{SPSCK}$ | SPSCK period | $4 \times t_{periph}$ | — | ns | 2 |
| 3 | $t_{Lead}$ | Enable lead time | 1 | — | $t_{periph}$ | — |
| 4 | $t_{Lag}$ | Enable lag time | 1 | — | $t_{periph}$ | — |
| 5 | $t_{WSPSCK}$ | Clock (SPSCK) high or low time | $t_{periph} - 30$ | — | ns | — |
| 6 | $t_{SU}$ | Data setup time (inputs) | 2 | — | ns | — |
| 7 | $t_{HI}$ | Data hold time (inputs) | 7 | — | ns | — |
| 8 | $t_a$ | Slave access time | — | $t_{periph}$ | ns | 3 |
| 9 | $t_{dis}$ | Slave MISO disable time | — | $t_{periph}$ | ns | 4 |
| 10 | $t_v$ | Data valid (after SPSCK edge) | — | 122 | ns | — |
| 11 | $t_{HO}$ | Data hold time (outputs) | 0 | — | ns | — |
| 12 | $t_{RI}$ | Rise time input | — | $t_{periph} - 25$ | ns | — |
| | $t_{FI}$ | Fall time input | | | | |
| 13 | $t_{RO}$ | Rise time output | — | 36 | ns | — |
| | $t_{FO}$ | Fall time output | | | | |

1. For SPI0, $f_{periph}$ is the bus clock ($f_{BUS}$).
2. $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state




NOTE: Not defined

**Figure 12. SPI slave mode timing (CPHA = 0)**




NOTE: Not defined

**Figure 13. SPI slave mode timing (CPHA = 1)**

## 3.8.2 Inter-Integrated Circuit Interface (I2C) timing

**Table 31. I2C timing**

| Characteristic | Symbol | Standard Mode | | Fast Mode | | Unit |
|---|---|---|---|---|---|---|
| | | Minimum | Maximum | Minimum | Maximum | |
| SCL Clock Frequency | $f_{SCL}$ | 0 | 100 | 0 | 400[1] | kHz |
| Hold time (repeated) START condition. After this period, the first clock pulse is generated. | $t_{HD}$; STA | 4 | — | 0.6 | — | µs |
| LOW period of the SCL clock | $t_{LOW}$ | 4.7 | — | 1.3 | — | µs |
| HIGH period of the SCL clock | $t_{HIGH}$ | 4 | — | 0.6 | — | µs |
| Set-up time for a repeated START condition | $t_{SU}$; STA | 4.7 | — | 0.6 | — | µs |
| Data hold time for I²C bus devices | $t_{HD}$; DAT | 0[2] | 3.45[3] | 0[4] | 0.9[2] | µs |
| Data set-up time | $t_{SU}$; DAT | 250[5] | — | 100[3], [6] | — | ns |
| Rise time of SDA and SCL signals | $t_r$ | — | 1000 | 20 +0.1$C_b$[7] | 300 | ns |
| Fall time of SDA and SCL signals | $t_f$ | — | 300 | 20 +0.1$C_b$[6] | 300 | ns |
| Set-up time for STOP condition | $t_{SU}$; STO | 4 | — | 0.6 | — | µs |
| Bus free time between STOP and START condition | $t_{BUF}$ | 4.7 | — | 1.3 | — | µs |
| Pulse width of spikes that must be suppressed by the input filter | $t_{SP}$ | N/A | N/A | 0 | 50 | ns |

1. The maximum SCL Clock Frequency in Fast mode with maximum bus loading can only achieved when using the High drive pins (see Voltage and current operating behaviors) or when using the Normal drive pins and VDD ≥ 2.7 V
2. The master mode I²C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
3. The maximum tHD; DAT must be met only if the device does not stretch the LOW period (tLOW) of the SCL signal.
4. Input signal Slew = 10 ns and Output Load = 50 pF
5. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
6. A Fast mode I²C bus device can be used in a Standard mode I2C bus system, but the requirement $t_{SU;\ DAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line $t_{rmax} + t_{SU;\ DAT} = 1000 + 250 = 1250$ ns (according to the Standard mode I²C bus specification) before the SCL line is released.
7. $C_b$ = total capacitance of the one bus line in pF.

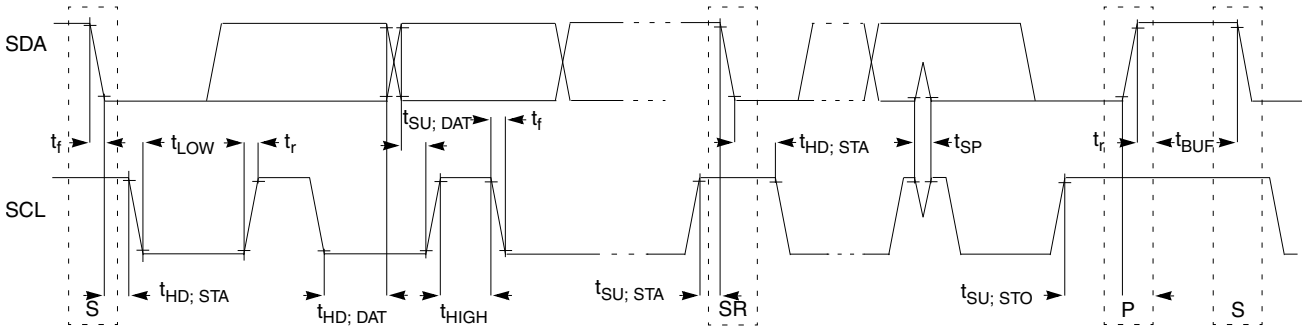



**Figure 14. Timing definition for fast and standard mode devices on the I²C bus**

### 3.8.3 UART

See General switching specifications.

# 4 Dimensions

## 4.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to **freescale.com** and perform a keyword search for the drawing's document number:

| If you want the drawing for this package | Then use this document number |
|---|---|
| 24-pin QFN | 98ASA00474D |
| 32-pin QFN | 98ASA00473D |
| 32-pin LQFP | 98ASH70029A |
| 48-pin LQFP | 98ASH00962A |

# 5 Pinout

## 5.1 KL04 signal multiplexing and pin assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

| 48 LQFP | 32 QFN | 32 LQFP | 24 QFN | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 1 | PTB6/ IRQ_2/ LPTMR0_ALT3 | DISABLED | DISABLED | PTB6/ IRQ_2/ LPTMR0_ALT3 | TPM0_CH3 | TPM_CLKIN1 |
| 2 | 2 | 2 | 2 | PTB7/ IRQ_3 | DISABLED | DISABLED | PTB7/ IRQ_3 | TPM0_CH2 | |
| 3 | – | – | – | PTA14 | DISABLED | DISABLED | PTA14 | | TPM_CLKIN0 |
| 4 | – | – | – | PTA15 | DISABLED | DISABLED | PTA15 | | CLKOUT |

| 48 LQFP | 32 QFN | 32 LQFP | 24 QFN | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 |
|---|---|---|---|---|---|---|---|---|---|
| 5 | 3 | 3 | 3 | VDD | VDD | VDD | | | |
| 6 | 4 | 4 | 3 | VREFH | VREFH | VREFH | | | |
| 7 | 5 | 5 | 4 | VREFL | VREFL | VREFL | | | |
| 8 | 6 | 6 | 4 | VSS | VSS | VSS | | | |
| 9 | 7 | 7 | 5 | PTA3 | EXTAL0 | EXTAL0 | PTA3 | I2C0_SCL | I2C0_SDA |
| 10 | 8 | 8 | 6 | PTA4/ LLWU_P0 | XTAL0 | XTAL0 | PTA4/ LLWU_P0 | I2C0_SDA | I2C0_SCL |
| 11 | — | — | — | VSS | VSS | VSS | | | |
| 12 | — | — | — | PTB18 | DISABLED | DISABLED | PTB18 | | |
| 13 | — | — | — | PTB19 | DISABLED | DISABLED | PTB19 | | |
| 14 | 9 | 9 | 7 | PTA5/ LLWU_P1/ RTC_CLK_IN | DISABLED | DISABLED | PTA5/ LLWU_P1/ RTC_CLK_IN | TPM0_CH5 | SPI0_SS_b |
| 15 | 10 | 10 | 8 | PTA6/ LLWU_P2 | DISABLED | DISABLED | PTA6/ LLWU_P2 | TPM0_CH4 | SPI0_MISO |
| 16 | 11 | 11 | — | PTB8 | ADC0_SE11 | ADC0_SE11 | PTB8 | TPM0_CH3 | |
| 17 | 12 | 12 | — | PTB9 | ADC0_SE10 | ADC0_SE10 | PTB9 | TPM0_CH2 | |
| 18 | — | — | — | PTA16/ IRQ_4 | DISABLED | DISABLED | PTA16/ IRQ_4 | | |
| 19 | — | — | — | PTA17/ IRQ_5 | DISABLED | DISABLED | PTA17/ IRQ_5 | | |
| 20 | — | — | — | PTA18/ IRQ_6 | DISABLED | DISABLED | PTA18/ IRQ_6 | | |
| 21 | 13 | 13 | 9 | PTB10 | ADC0_SE9 | ADC0_SE9 | PTB10 | TPM0_CH1 | |
| 22 | 14 | 14 | 10 | PTB11 | ADC0_SE8 | ADC0_SE8 | PTB11 | TPM0_CH0 | |
| 23 | 15 | 15 | 11 | PTA7/ IRQ_7/ LLWU_P3 | ADC0_SE7 | ADC0_SE7 | PTA7/ IRQ_7/ LLWU_P3 | SPI0_MISO | SPI0_MOSI |
| 24 | 16 | 16 | 12 | PTB0/ IRQ_8/ LLWU_P4 | ADC0_SE6 | ADC0_SE6 | PTB0/ IRQ_8/ LLWU_P4 | EXTRG_IN | SPI0_SCK |
| 25 | 17 | 17 | 13 | PTB1/ IRQ_9 | ADC0_SE5/ CMP0_IN3 | ADC0_SE5/ CMP0_IN3 | PTB1/ IRQ_9 | UART0_TX | UART0_RX |
| 26 | 18 | 18 | 14 | PTB2/ IRQ_10/ LLWU_P5 | ADC0_SE4 | ADC0_SE4 | PTB2/ IRQ_10/ LLWU_P5 | UART0_RX | UART0_TX |
| 27 | 19 | 19 | 15 | PTA8 | ADC0_SE3 | ADC0_SE3 | PTA8 | | |
| 28 | 20 | 20 | 16 | PTA9 | ADC0_SE2 | ADC0_SE2 | PTA9 | | |
| 29 | — | — | — | PTB20 | DISABLED | DISABLED | PTB20 | | |
| 30 | — | — | — | VSS | VSS | VSS | | | |
| 31 | — | — | — | VDD | VDD | VDD | | | |
| 32 | — | — | — | PTB14/ IRQ_11 | DISABLED | DISABLED | PTB14/ IRQ_11 | EXTRG_IN | |

| 48 LQFP | 32 QFN | 32 LQFP | 24 QFN | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 |
|---|---|---|---|---|---|---|---|---|---|
| 33 | 21 | 21 | — | PTA10/ IRQ_12 | DISABLED | DISABLED | PTA10/ IRQ_12 | | |
| 34 | 22 | 22 | — | PTA11/ IRQ_13 | DISABLED | DISABLED | PTA11/ IRQ_13 | | |
| 35 | 23 | 23 | 17 | PTB3/ IRQ_14 | DISABLED | DISABLED | PTB3/ IRQ_14 | I2C0_SCL | UART0_TX |
| 36 | 24 | 24 | 18 | PTB4/ IRQ_15/ LLWU_P6 | DISABLED | DISABLED | PTB4/ IRQ_15/ LLWU_P6 | I2C0_SDA | UART0_RX |
| 37 | 25 | 25 | 19 | PTB5/ IRQ_16 | NMI_b | ADC0_SE1/ CMP0_IN1 | PTB5/ IRQ_16 | TPM1_CH1 | NMI_b |
| 38 | 26 | 26 | 20 | PTA12/ IRQ_17/ LPTMR0_ALT2 | ADC0_SE0/ CMP0_IN0 | ADC0_SE0/ CMP0_IN0 | PTA12/ IRQ_17/ LPTMR0_ALT2 | TPM1_CH0 | TPM_CLKIN0 |
| 39 | 27 | 27 | — | PTA13 | DISABLED | DISABLED | PTA13 | | |
| 40 | 28 | 28 | — | PTB12 | DISABLED | DISABLED | PTB12 | | |
| 41 | — | — | — | PTA19 | DISABLED | DISABLED | PTA19 | | SPI0_SS_b |
| 42 | — | — | — | PTB15 | DISABLED | DISABLED | PTB15 | SPI0_MOSI | SPI0_MISO |
| 43 | — | — | — | PTB16 | DISABLED | DISABLED | PTB16 | SPI0_MISO | SPI0_MOSI |
| 44 | — | — | — | PTB17 | DISABLED | DISABLED | PTB17 | TPM_CLKIN1 | SPI0_SCK |
| 45 | 29 | 29 | 21 | PTB13 | ADC0_SE13 | ADC0_SE13 | PTB13 | TPM1_CH1 | RTC_CLKOUT |
| 46 | 30 | 30 | 22 | PTA0/ IRQ_0/ LLWU_P7 | SWD_CLK | ADC0_SE12/ CMP0_IN2 | PTA0/ IRQ_0/ LLWU_P7 | TPM1_CH0 | SWD_CLK |
| 47 | 31 | 31 | 23 | PTA1/ IRQ_1/ LPTMR0_ALT1 | RESET_b | DISABLED | PTA1/ IRQ_1/ LPTMR0_ALT1 | TPM_CLKIN0 | RESET_b |
| 48 | 32 | 32 | 24 | PTA2 | SWD_DIO | DISABLED | PTA2 | CMP0_OUT | SWD_DIO |

## 5.2 KL04 pinouts

The following figures show the pinout diagrams for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see KL04 signal multiplexing and pin assignments.

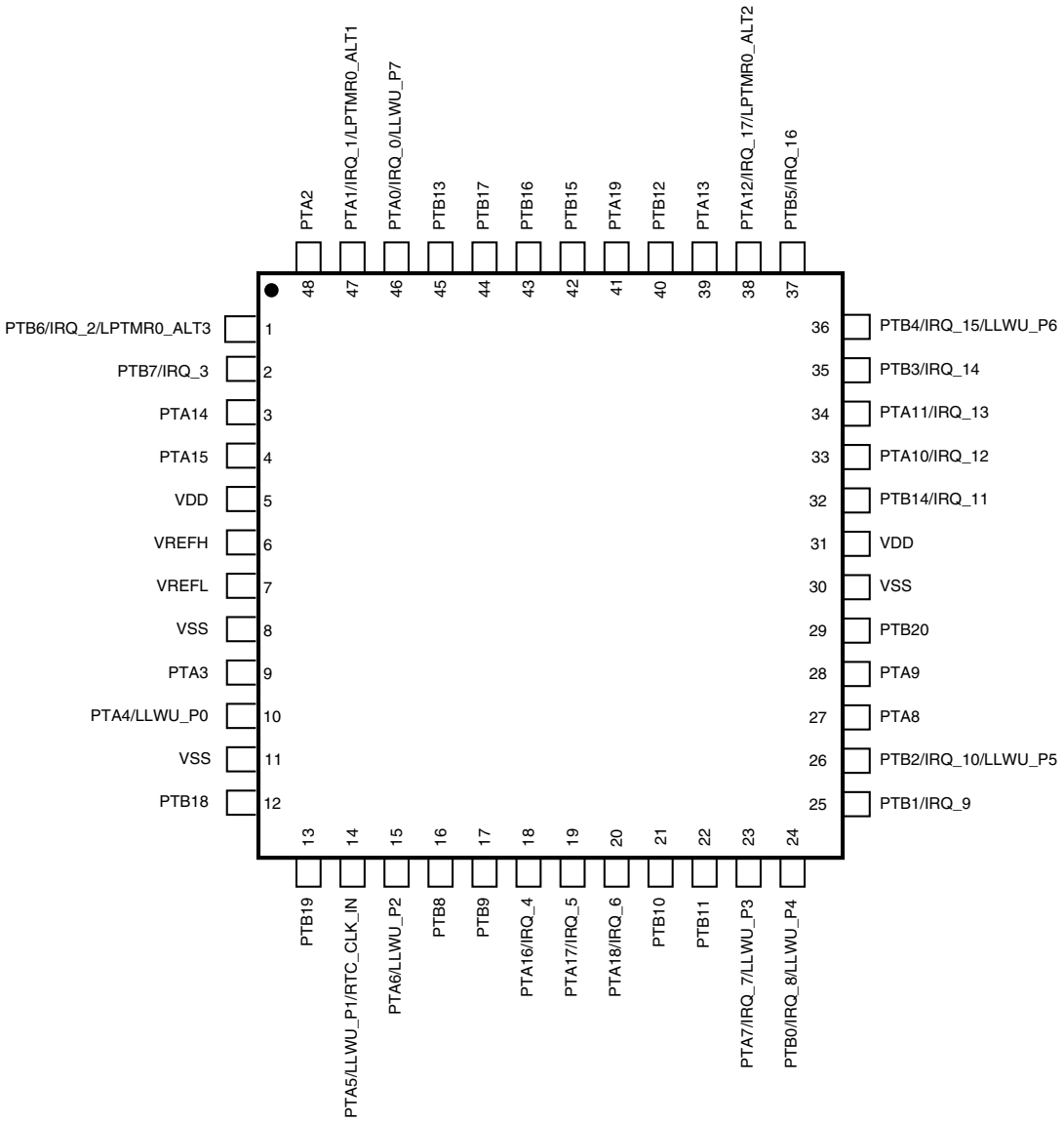



**Figure 15. KL04 48-pin LQFP pinout diagram**

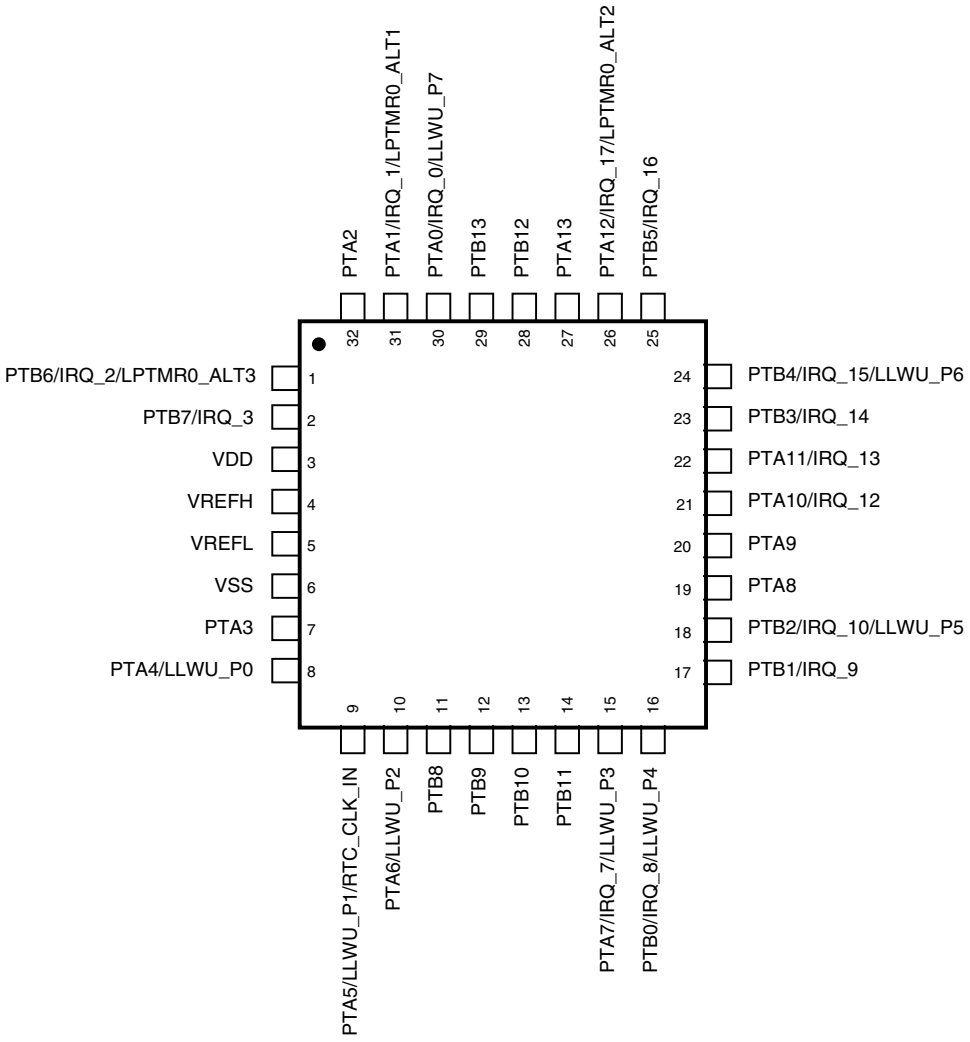



**Figure 16. KL04 32-pin LQFP pinout diagram**

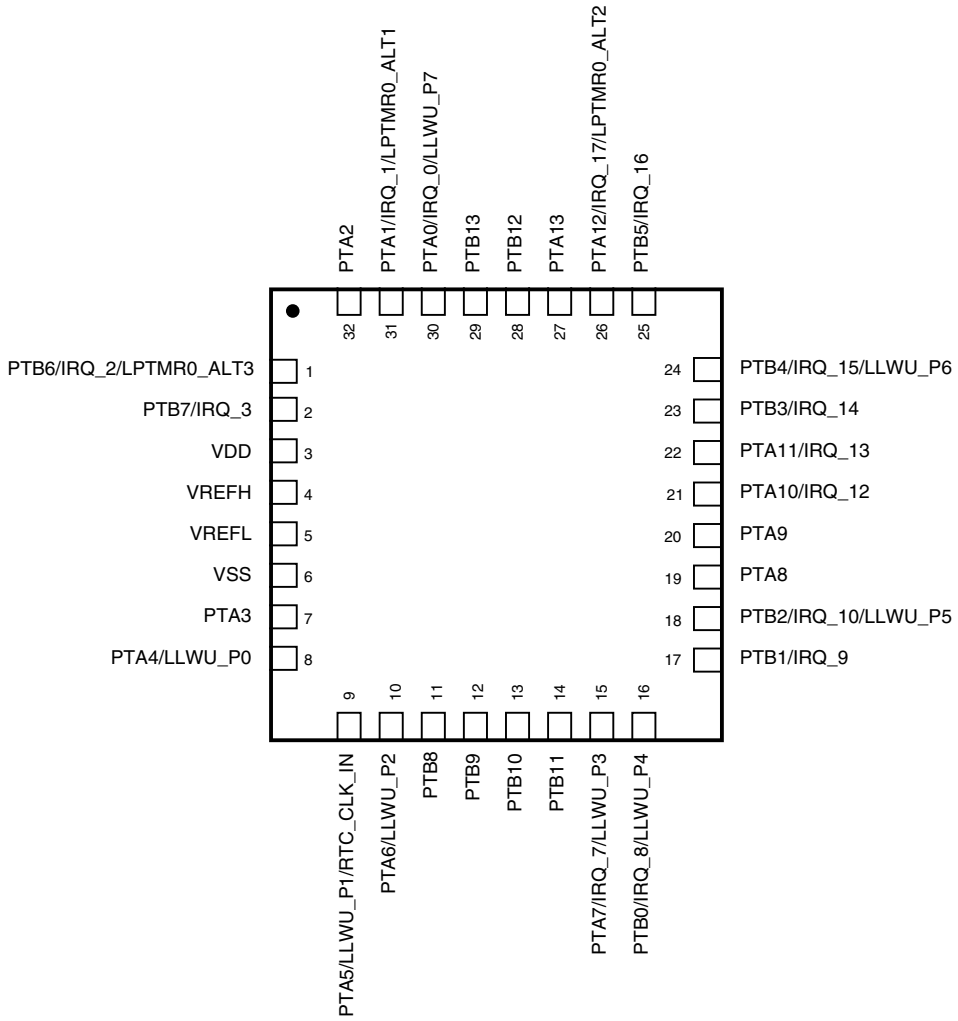



**Figure 17. KL04 32-pin QFN pinout diagram**

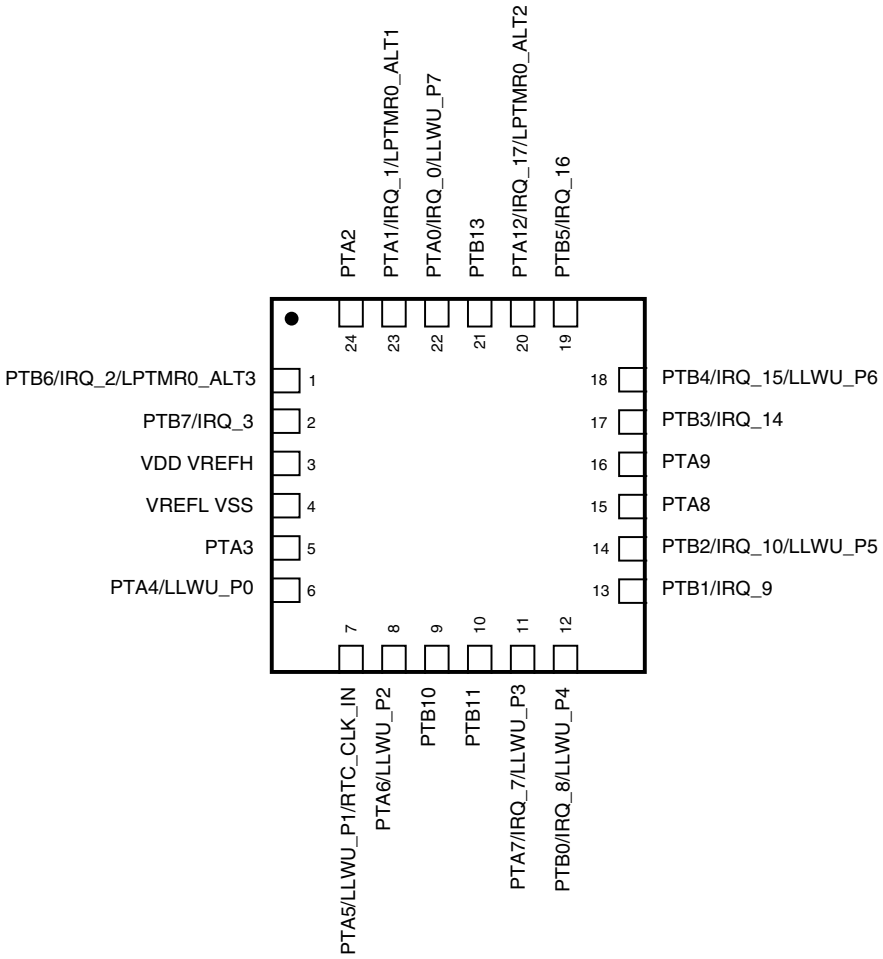



**Figure 18. KL04 24-pin QFN pinout diagram**

# 6 Ordering parts

## 6.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to **freescale.com** and perform a part number search for the following device numbers: PKL04 and MKL04

# 7 Part identification

## 7.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

## 7.2 Format

Part numbers for this device have the following format:

Q KL## A FFF R T PP CC N

## 7.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

**Table 32. Part number fields descriptions**

| Field | Description | Values |
|---|---|---|
| Q | Qualification status | • M = Fully qualified, general market flow<br>• P = Prequalification |
| KL## | Kinetis family | • KL04 |
| A | Key attribute | • Z = Cortex-M0+ |
| FFF | Program flash memory size | • 8 = 8 KB<br>• 16 = 16 KB<br>• 32 = 32 KB |
| R | Silicon revision | • (Blank) = Main<br>• A = Revision after main |
| T | Temperature range (°C) | • V = –40 to 105 |
| PP | Package identifier | • FK = 24 QFN (4 mm x 4 mm)<br>• LC = 32 LQFP (7 mm x 7 mm)<br>• FM = 32 QFN (5 mm x 5 mm)<br>• LF = 48 LQFP (7 mm x 7 mm) |
| CC | Maximum CPU frequency (MHz) | • 4 = 48 MHz |
| N | Packaging type | • R = Tape and reel<br>• (Blank) = Trays |

## 7.4 Example

This is an example part number:

# 8 Terminology and guidelines

## 8.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

### 8.1.1 Example

This is an example of an operating requirement:

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$ | 1.0 V core supply voltage | 0.9 | 1.1 | V |

## 8.2 Definition: Operating behavior

Unless otherwise specified, an *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

## 8.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

### 8.3.1 Example

This is an example of an attribute:

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| CIN_D | Input capacitance: digital pins | — | 7 | pF |

## 8.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

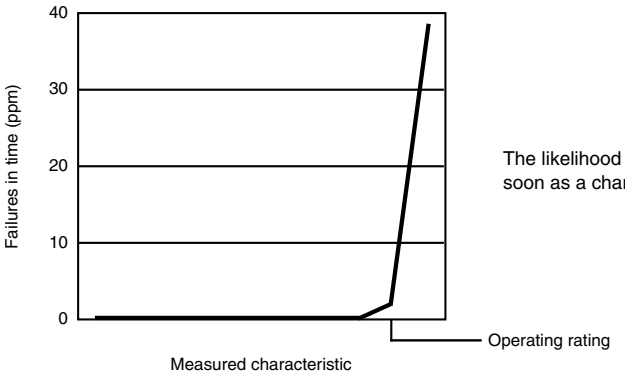
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

### 8.4.1 Example

This is an example of an operating rating:

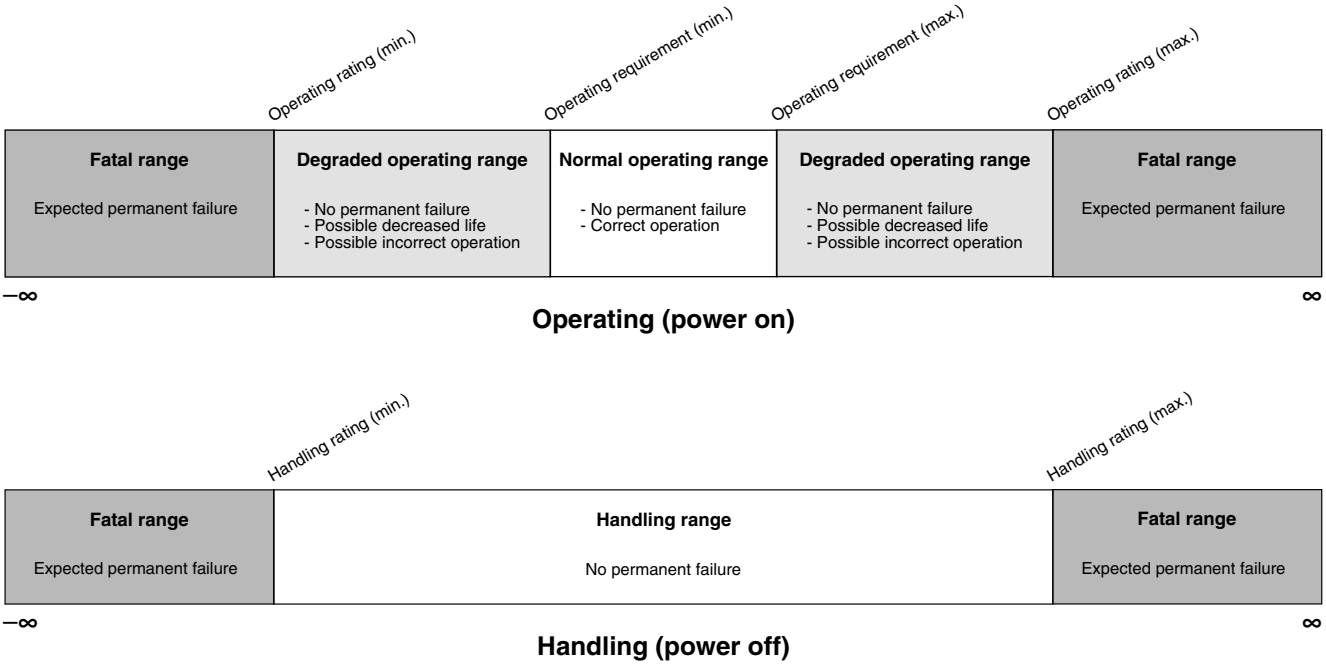
| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$ | 1.0 V core supply voltage | –0.3 | 1.2 | V |

## 8.5 Result of exceeding a rating




The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

## 8.6 Relationship between ratings and operating requirements




## 8.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

## 8.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

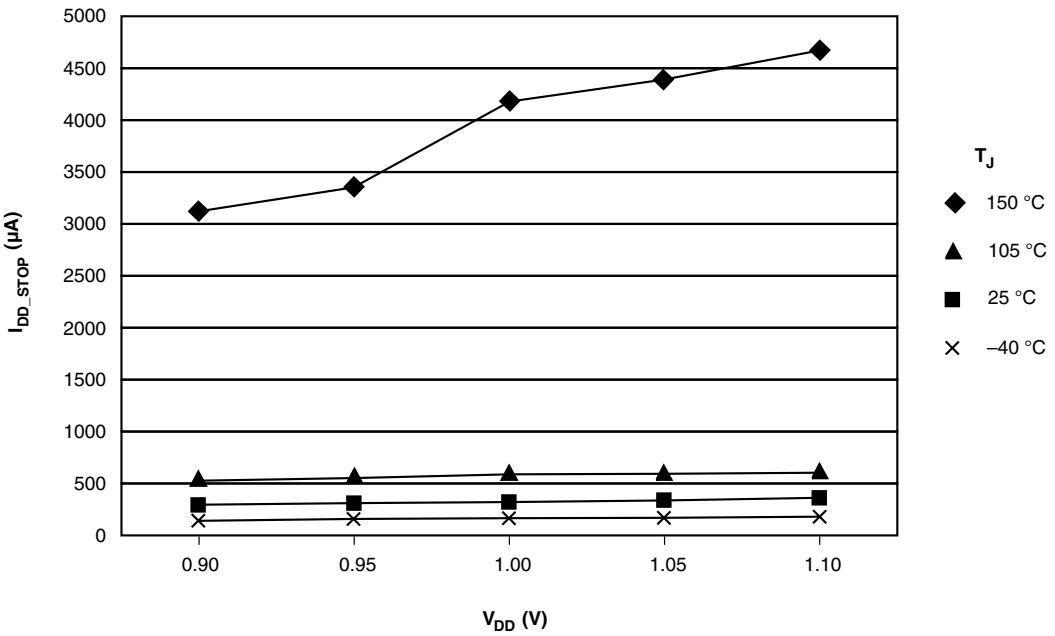
### 8.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $I_{WP}$ | Digital I/O weak pullup/pulldown current | 10 | 70 | 130 | µA |

### 8.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:




## 8.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

**Table 33. Typical value conditions**

| Symbol | Description | Value | Unit |
|---|---|---|---|
| $T_A$ | Ambient temperature | 25 | °C |
| $V_{DD}$ | 3.3 V supply voltage | 3.3 | V |

# 9 Revision history

The following table provides a revision history for this document.

**Table 34. Revision history**

| Rev. No. | Date | Substantial Changes |
|---|---|---|
| 2 | 9/2012 | Initial public release. |
| 3 | 11/2012 | Completed all the TBDs. |
| 4 | 3/2014 | • Updated the front page and restructured the chapters<br>• Added a note to the $I_{LAT}$ in the ESD handling ratings<br>• Updated Voltage and current operating ratings<br>• Added $V_{ODPU}$ in the Voltage and current operating requirements<br>• Updated Voltage and current operating behaviors<br>• Updated Power mode transition operating behaviors<br>• Updated Power consumption operating behaviors<br>• Updated Capacitance attributes<br>• Updated footnote in the Device clock specifications<br>• Updated $t_{ersall}$ in the Flash timing specifications — commands<br>• Updated Temp sensor slope and voltage and added a note to them in the 12-bit ADC electrical characteristics<br>• Removed $T_A$ in the 12-bit DAC operating requirements<br>• Added Inter-Integrated Circuit Interface (I2C) timing |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