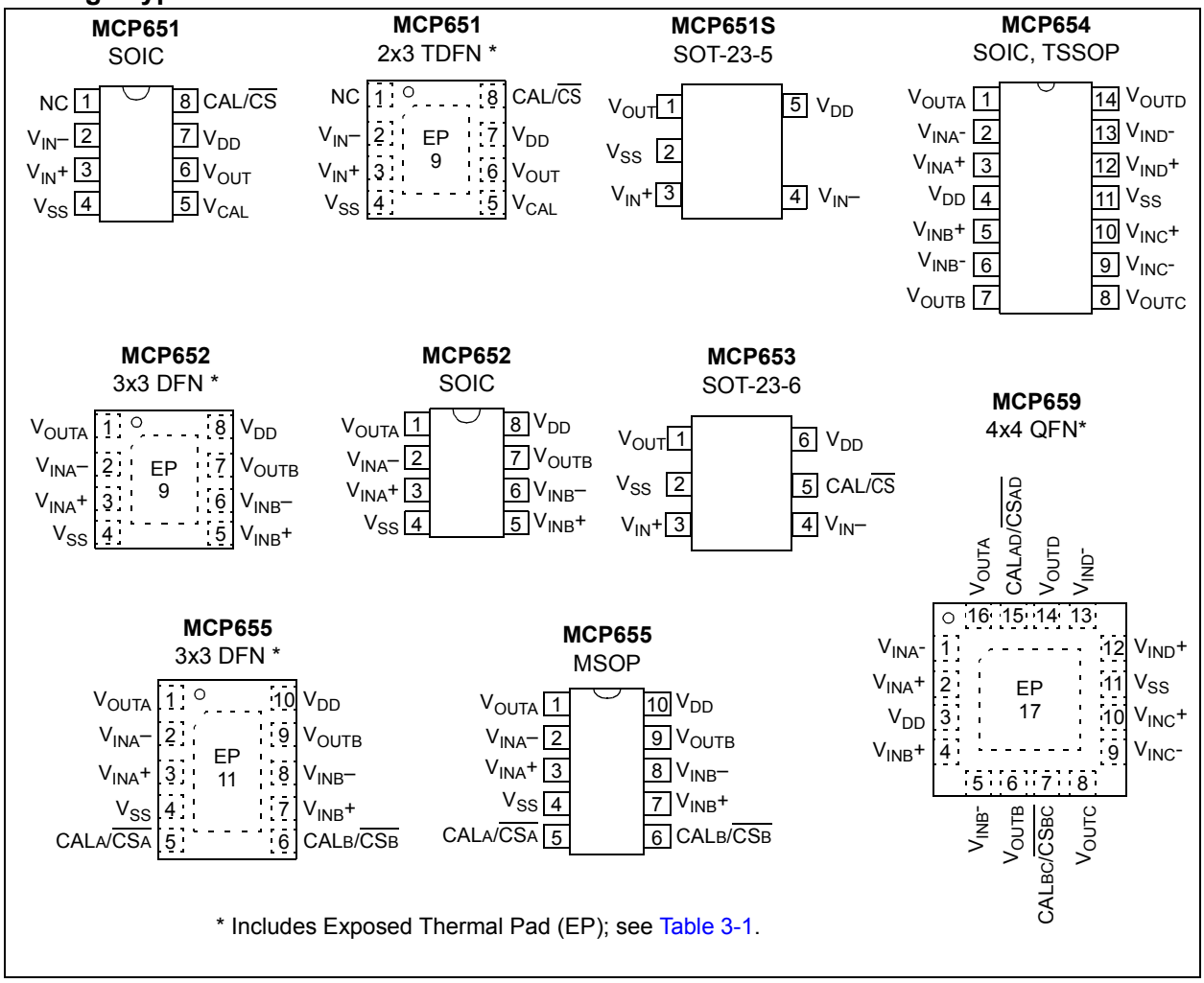
Package Types



* Includes Exposed Thermal Pad (EP); see Table 3-1.

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1.0 ELECTRICAL CHARACTERISTICS

1.1 Absolute Maximum Ratings †

$V_{DD} - V_{SS}$ 6.5V
Current at Input Pins .....±2 mA
Analog Inputs (V_{IN}+ and V_{IN}–) †† . V_{SS} – 1.0V to V_{DD} + 1.0V
All other Inputs and Outputs ..... V_{SS} – 0.3V to V_{DD} + 0.3V
Difference Input voltage ..... $|V_{DD} - V_{SS}|$
Output Short Circuit Current .....Continuous
Current at Output and Supply Pins .....±150 mA
Storage Temperature .....-65°C to +150°C
Max. Junction Temperature .....+150°C
ESD protection on all pins (HBM, MM) .....≥ 1 kV, 200V

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† See **Section 4.2.2 "Input Voltage and Current Limits"**.

1.2 Specifications

TABLE 1-1: DC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 1 kΩ to V_L and CAL/$\overline{CS}$ = V_{SS} (refer to Figure 1-2).

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Input Offset						
Input Offset Voltage	V_{OS}	-200	—	+200	µV	After calibration **(Note 1)**
Input Offset Voltage Trim Step	V_{OSTRM}	—	37	200	µV	
Input Offset Voltage Drift	$\Delta V_{OS}/\Delta T_A$	—	±2.5	—	µV/°C	T_A= -40°C to +125°C
Power Supply Rejection Ratio	PSRR	61	76	—	dB	
Input Current and Impedance						
Input Bias Current	I_B	—	6	—	pA	
Across Temperature	I_B	—	130	—	pA	T_A= +85°C
Across Temperature	I_B	—	1700	5,000	pA	T_A= +125°C
Input Offset Current	I_{OS}	—	±1	—	pA	
Common Mode Input Impedance	Z_{CM}	—	10^{13}||9	—	Ω||pF	
Differential Input Impedance	Z_{DIFF}	—	10^{13}||2	—	Ω||pF	
Common Mode						
Common Mode Input Voltage Range	V_{CMR}	V_{SS} – 0.3	—	V_{DD} – 1.3	V	**(Note 2)**
Common Mode Rejection Ratio	CMRR	65	81	—	dB	V_{DD} = 2.5V, V_{CM} = -0.3 to 1.2V
	CMRR	68	84	—	dB	V_{DD} = 5.5V, V_{CM} = -0.3 to 4.2V
Open-Loop Gain						
DC Open-Loop Gain (large signal)	A_{OL}	88	114	—	dB	V_{DD} = 2.5V, V_{OUT} = 0.3V to 2.2V
	A_{OL}	94	123	—	dB	V_{DD} = 5.5V, V_{OUT} = 0.3V to 5.2V
Output						
Maximum Output Voltage Swing	V_{OL}, V_{OH}	V_{SS} + 25	—	V_{DD} – 25	mV	V_{DD} = 2.5V, G = +2, 0.5V Input Overdrive
	V_{OL}, V_{OH}	V_{SS} + 50	—	V_{DD} – 50	mV	V_{DD} = 5.5V, G = +2, 0.5V Input Overdrive
Output Short-Circuit Current	I_{SC}	±50	±95	±145	mA	V_{DD} = 2.5V **(Note 3)**
	I_{SC}	±50	±100	±150	mA	V_{DD} = 5.5V **(Note 3)**

Note 1: Describes the offset (under the specified conditions) right after power-up, or just after the CAL/$\overline{CS}$ pin is toggled. Thus, 1/f noise effects (an apparent wander in V_{OS}; see Figure 2-35) are not included.
2: See Figure 2-6 and Figure 2-7 for temperature effects.
3: The I_{SC} specifications are for design guidance only; they are not tested.

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TABLE 1-1: DC ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 1 kΩ to V_L and CAL/$\overline{CS}$ = V_{SS} (refer to Figure 1-2).

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Calibration Input						
Calibration Input Voltage Range	V_{CALRNG}	V_{SS} + 0.1	—	V_{DD} – 1.4	mV	V_{CAL} pin externally driven
Internal Calibration Voltage	V_{CAL}	0.31V_{DD}	0.33V_{DD}	0.35V_{DD}		V_{CAL} pin open
Input Impedance	Z_{CAL}	—	100 || 5	—	kΩ||pF	
Power Supply						
Supply Voltage	V_{DD}	2.5	—	5.5	V	
Quiescent Current per Amplifier	I_Q	3	6	9	mA	I_O = 0
POR Input Threshold, Low	V_{PRL}	1.15	1.40	—	V	
POR Input Threshold, High	V_{PRH}	—	1.40	1.65	V	

Note 1: Describes the offset (under the specified conditions) right after power-up, or just after the CAL/$\overline{CS}$ pin is toggled. Thus, 1/f noise effects (an apparent wander in V_{OS}; see Figure 2-35) are not included.

2: See Figure 2-6 and Figure 2-7 for temperature effects.

3: The I_{SC} specifications are for design guidance only; they are not tested.

TABLE 1-2: AC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = 25°C, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 1 kΩ to V_L, C_L = 20 pF and CAL/$\overline{CS}$ = V_{SS} (refer to Figure 1-2).

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
AC Response						
Gain-Bandwidth Product	GBWP	—	50	—	MHz	
Phase Margin	PM	—	65	—	°	G = +1
Open-Loop Output Impedance	R_{OUT}	—	20	—	Ω	
AC Distortion						
Total Harmonic Distortion plus Noise	THD+N	—	0.0012	—	%	G = +1, V_{OUT} = 4V_{P-P}, f = 1 kHz, V_{DD} = 5.5V, BW = 80 kHz
Step Response						
Rise Time, 10% to 90%	t_r	—	6	—	ns	G = +1, V_{OUT} = 100 mV_{P-P}
Slew Rate	SR	—	30	—	V/µs	G = +1
Noise						
Input Noise Voltage	E_{ni}	—	17	—	µV_{P-P}	f = 0.1 Hz to 10 Hz
Input Noise Voltage Density	e_{ni}	—	7.5	—	nV/√Hz	f = 1 MHz
Input Noise Current Density	i_{ni}		4	—	fA/√Hz	f = 1 kHz

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TABLE 1-3: DIGITAL ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = 25°C, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 1 kΩ to V_L, C_L = 20 pF and CAL/$\overline{CS}$ = V_{SS} (refer to Figure 1-1 and Figure 1-2).

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
CAL/$\overline{CS}$ Low Specifications						
CAL/$\overline{CS}$ Logic Threshold, Low	V_{IL}	V_{SS}	—	0.2V_{DD}	V	
CAL/$\overline{CS}$ Input Current, Low	I_{CSL}	—	0	—	nA	CAL/$\overline{CS}$ = 0V
CAL/$\overline{CS}$ High Specifications						
CAL/$\overline{CS}$ Logic Threshold, High	V_{IH}	0.8V_{DD}		V_{DD}	V	
CAL/$\overline{CS}$ Input Current, High	I_{CSH}	—	0.7	—	µA	CAL/$\overline{CS}$ = V_{DD}
GND Current	I_{SS}	-3.5	-1.8	—	µA	Single, CAL/$\overline{CS}$ = V_{DD} = 2.5V
	I_{SS}	-8	-4	—	µA	Single, CAL/$\overline{CS}$ = V_{DD} = 5.5V
	I_{SS}	-5	-2.5	—	µA	Dual, CAL/$\overline{CS}$ = V_{DD} = 2.5V
	I_{SS}	-10	-5	—	µA	Dual, CAL/$\overline{CS}$ = V_{DD} = 5.5V
CAL/$\overline{CS}$ Internal Pull-Down Resistor	R_{PD}	—	5	—	MΩ	
Amplifier Output Leakage	$I_{O(LEAK)}$	—	50	—	nA	CAL/$\overline{CS}$ = V_{DD}
POR Dynamic Specifications						
V_{DD} Low to Amplifier Off Time (output goes High Z)	t_{POFF}	—	200	—	ns	G = +1 V/V, V_L = V_{SS}, V_{DD} = 2.5V to 0V step to V_{OUT} = 0.1 (2.5V)
V_{DD} High to Amplifier On Time (including calibration)	t_{PON}	100	200	300	ms	G = +1 V/V, V_L = V_{SS}, V_{DD} = 0V to 2.5V step to V_{OUT} = 0.9 (2.5V)
CAL/$\overline{CS}$ Dynamic Specifications						
CAL/$\overline{CS}$ Input Hysteresis	V_{HYST}	—	0.25	—	V	
CAL/$\overline{CS}$ Setup Time (between CAL/$\overline{CS}$ edges)	t_{CSU}	1	—	—	µs	G = +1 V/V, V_L = V_{SS} **(Notes 2, 3, 4)** CAL/$\overline{CS}$ = 0.8V_{DD} to V_{OUT} = 0.1 (V_{DD}/2)
CAL/$\overline{CS}$ High to Amplifier Off Time (output goes High Z)	t_{COFF}	—	200	—	ns	G = +1 V/V, V_L = V_{SS}, CAL/$\overline{CS}$ = 0.8V_{DD} to V_{OUT} = 0.1 (V_{DD}/2)
CAL/$\overline{CS}$ Low to Amplifier On Time (including calibration)	t_{CON}	—	3	4	ms	G = +1 V/V, V_L = V_{SS}, MCP651 and MCP655, CAL/$\overline{CS}$ = 0.2V_{DD} to V_{OUT} = 0.9 (V_{DD}/2)
	t_{CON}	—	6	8	ms	G = +1 V/V, V_L = V_{SS}, MCP659, CAL/$\overline{CS}$ = 0.2V_{DD} to V_{OUT} = 0.9 (V_{DD}/2)

Note 1: The MCP652 single, MCP653 single, MCP655 dual and MCP659 quad have their CAL/$\overline{CS}$ inputs internally pulled down to V_{SS} (0V).

2: This time ensures that the internal logic recognizes the edge. However, for the rising edge case, if CAL/$\overline{CS}$ is raised before the calibration is complete, the calibration will be aborted and the part will return to Low-Power mode.

3: For the MCP655 dual, there is an additional constraint. CALA/$\overline{CS}$A and CALB/$\overline{CS}$B can be toggled simultaneously (within a time much smaller than t_{CSU}) to make both op amps perform the same function simultaneously. If they are toggled independently, then CALA/$\overline{CS}$A (CALB/$\overline{CS}$B) cannot be allowed to toggle while op amp B (op amp A) is in Calibration mode; allow more than the maximum t_{CON} time (4 ms) before the other side is toggled.

4: For the MCP659 quad, there is an additional constraint. CALAD/$\overline{CS}$AD and CALBC/$\overline{CS}$BC can be toggled simultaneously (within a time much smaller than t_{CSU}) to make all four op amps perform the same function simultaneously, and the maximum t_{CON} time is approximately doubled (8 ms). If they are toggled independently, then CALAD/$\overline{CS}$AD (CALBC/$\overline{CS}$BC) cannot be allowed to toggle while op amps B and C (op amps A and D) are in Calibration mode; allow more than the maximum t_{CON} time (8 ms) before the other side is toggled.

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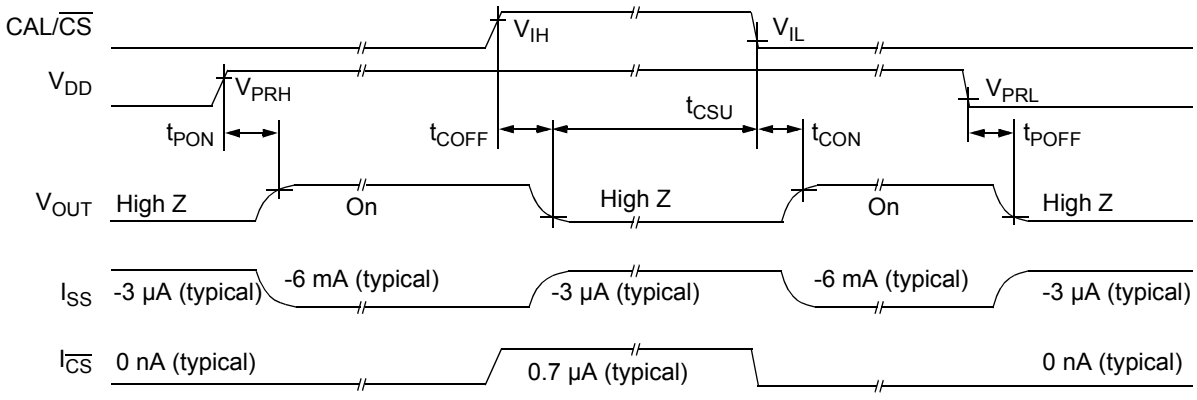
TABLE 1-4: TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, all limits are specified for: V_{DD} = +2.5V to +5.5V, V_{SS} = GND.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	**(Note 1)**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 5L-2×3 SOT	θ_{JA}	—	220.7	—	°C/W	
Thermal Resistance, 6L-2×3 SOT	θ_{JA}	—	190.5	—	°C/W	
Thermal Resistance, 8L-2×3 TDFN	θ_{JA}	—	52.5	—	°C/W	
Thermal Resistance, 8L-3×3 DFN	θ_{JA}	—	63	—	°C/W	**(Note 2)**
Thermal Resistance, 8L-SOIC	θ_{JA}	—	163	—	°C/W	
Thermal Resistance, 10L-3×3 DFN	θ_{JA}	—	71	—	°C/W	**(Note 2)**
Thermal Resistance, 10L-MSOP	θ_{JA}	—	202	—	°C/W	
Thermal Resistance, 14L-SOIC	θ_{JA}	—	95.3	—	°C/W	
Thermal Resistance, 14L-TSSOP	θ_{JA}	—	100	—	°C/W	
Thermal Resistance, 16L-4x4-QFN	θ_{JA}	—	46	—	°C/W	**(Note 2)**

Note 1: Operation must not cause T_J to exceed Maximum Junction Temperature specification (150°C).

2: Measured on a standard JC51-7, four-layer printed circuit board with ground plane and vias.

1.3 Timing Diagram



Note: For the MCP655 dual and the MCP659 quad, there is an additional constraint on toggling the two CAL/$\overline{CS}$ pins close together; see the T_{CON} specification in Table 1-3.

FIGURE 1-1: *Timing Diagram.*

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1.4 Test Circuits

The circuit used for most DC and AC tests is shown in Figure 1-2. This circuit can independently set V_{CM} and V_{OUT}; see Equation 1-1. Note that V_{CM} is not the circuit's Common mode voltage ((V_P + V_M)/2), and that V_{OST} includes V_{OS} plus the effects (on the input offset error, V_{OST}) of temperature, CMRR, PSRR and A_{OL}.

EQUATION 1-1:

$$G_{DM} = R_F/R_G$$
$$V_{CM} = (V_P + V_{DD}/2)/2$$
$$V_{OST} = V_{IN-} - V_{IN+}$$
$$V_{OUT} = (V_{DD}/2) + (V_P - V_M) + V_{OST}(1 + G_{DM})$$

Where:

G_{DM}	=	Differential Mode Gain	(V/V)
V_{CM}	=	Op Amp's Common Mode Input Voltage	(V)
V_{OST}	=	Op Amp's Total Input Offset Voltage	(mV)

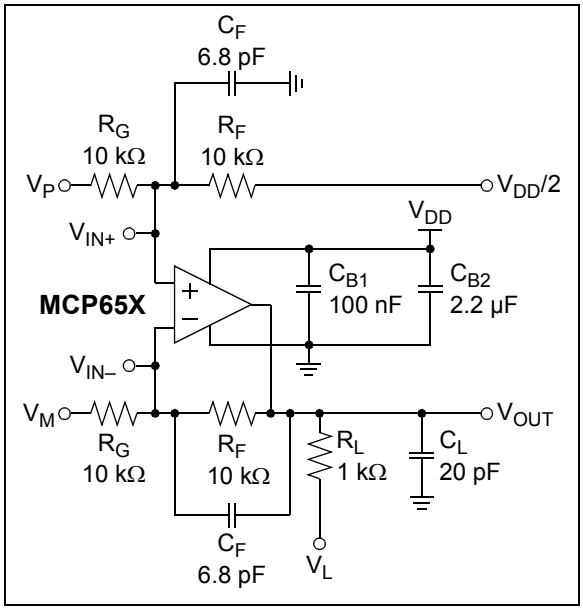

FIGURE 1-2: *AC and DC Test Circuit for Most Specifications.*

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2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 1 kΩ to V_L, C_L = 20 pF, and CAL/$\overline{CS}$ = V_{SS}.

2.1 DC Signal Inputs

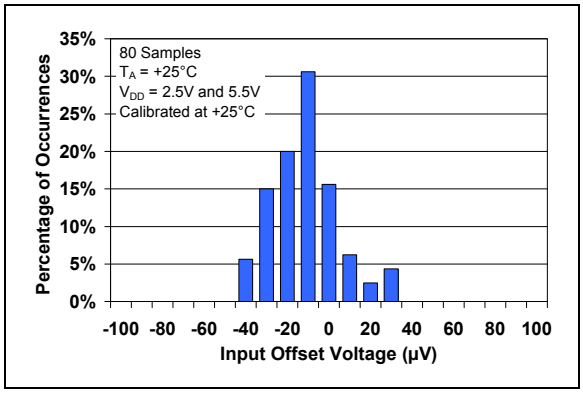

FIGURE 2-1: *Input Offset Voltage.*

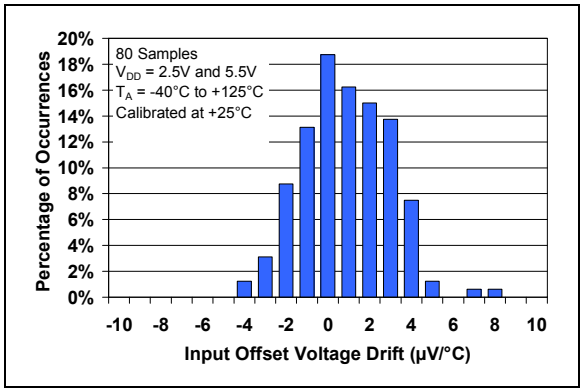

FIGURE 2-2: *Input Offset Voltage Drift.*

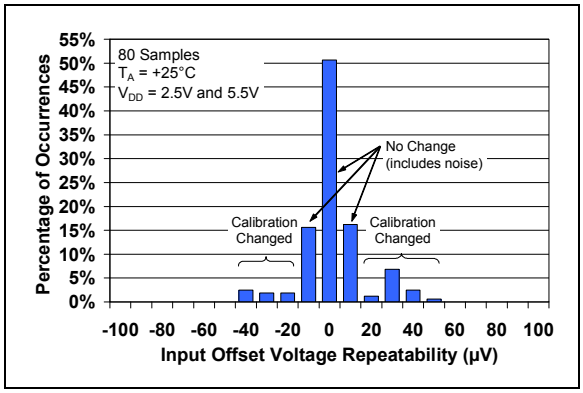

FIGURE 2-3: *Input Offset Voltage Repeatability (repeated calibration).*

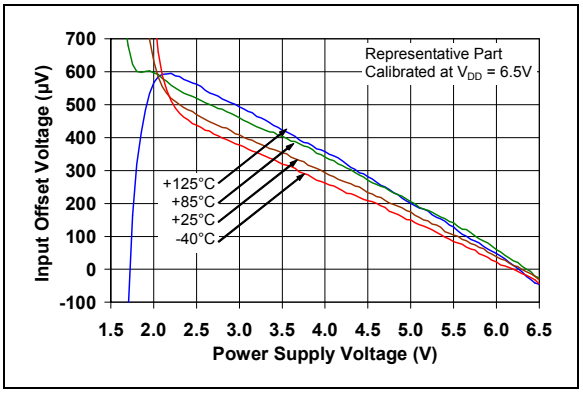

FIGURE 2-4: *Input Offset Voltage vs. Power Supply Voltage.*

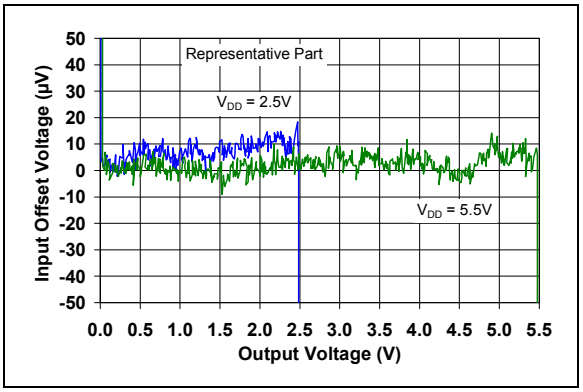

FIGURE 2-5: *Input Offset Voltage vs. Output Voltage.*

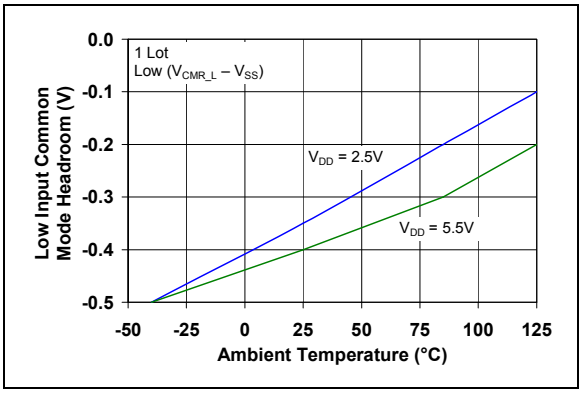

FIGURE 2-6: *Low-Input Common Mode Voltage Headroom vs. Ambient Temperature.*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 1 kΩ to V_L, C_L = 20 pF, and CAL/$\overline{CS}$ = V_{SS}.

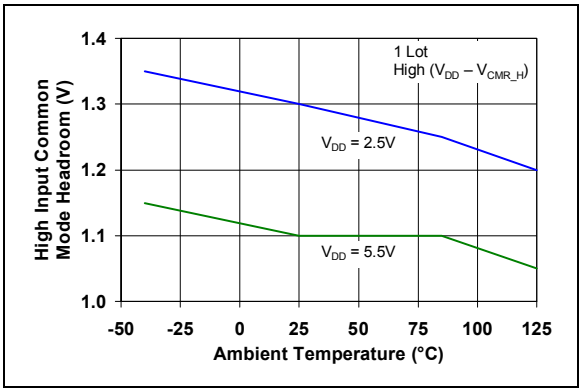

FIGURE 2-7: *High-Input Common Mode Voltage Headroom vs. Ambient Temperature.*

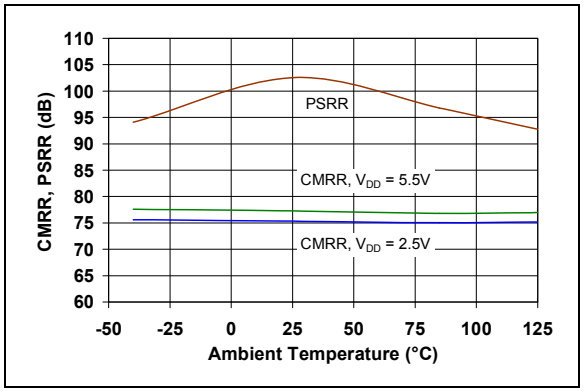

FIGURE 2-10: *CMRR and PSRR vs. Ambient Temperature.*

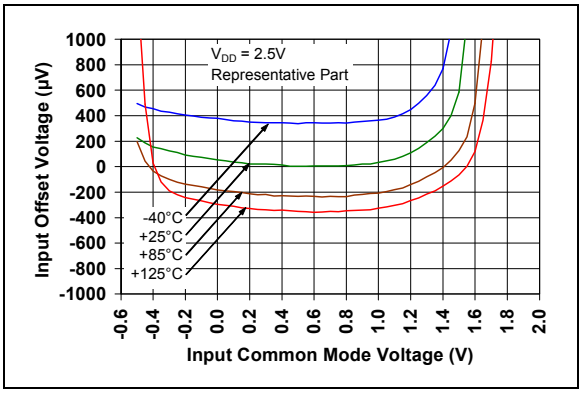

FIGURE 2-8: *Input Offset Voltage vs. Common Mode Voltage with V_{DD} = 2.5V.*

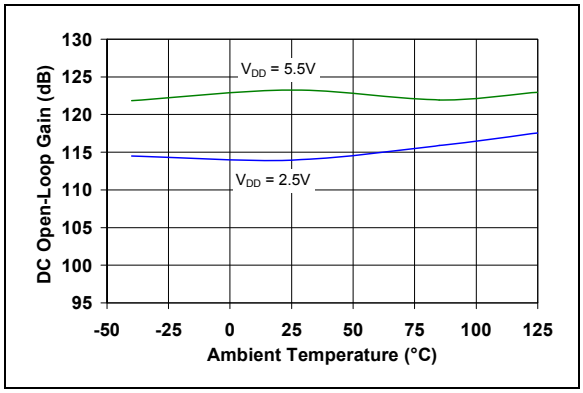

FIGURE 2-11: *DC Open-Loop Gain vs. Ambient Temperature.*

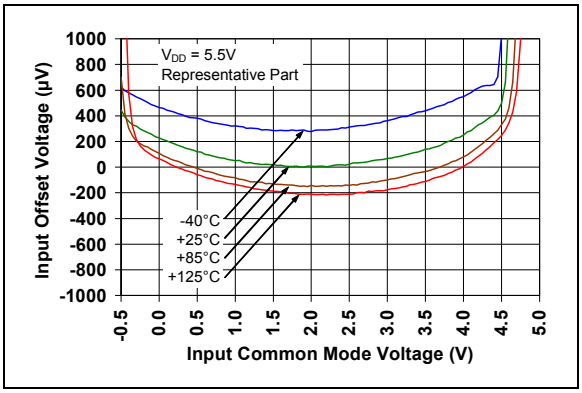

FIGURE 2-9: *Input Offset Voltage vs. Common Mode Voltage with V_{DD} = 5.5V.*

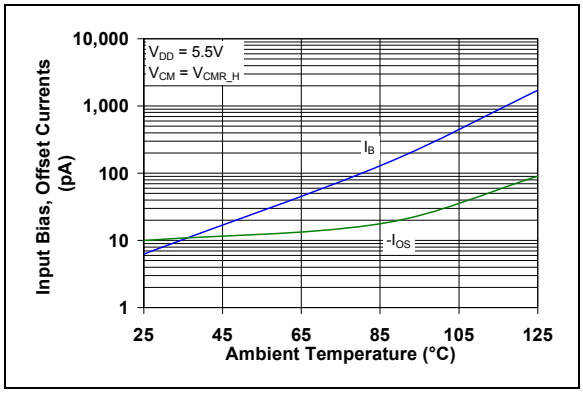

FIGURE 2-12: *Input Bias and Offset Currents vs. Ambient Temperature with V_{DD} = +5.5V.*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 1 kΩ to V_L, C_L = 20 pF, and CAL/$\overline{CS}$ = V_{SS}.

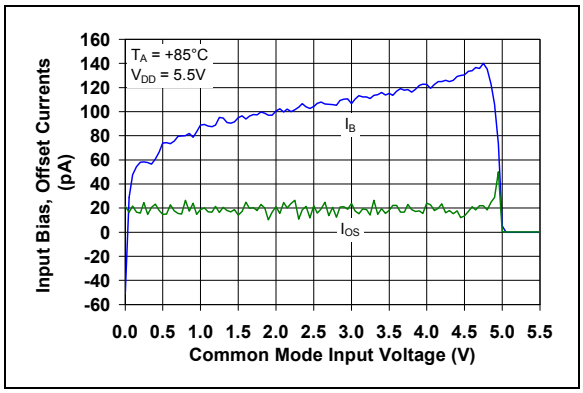

FIGURE 2-13: *Input Bias and Offset Currents vs. Common Mode Input Voltage with T_A = +85°C.*

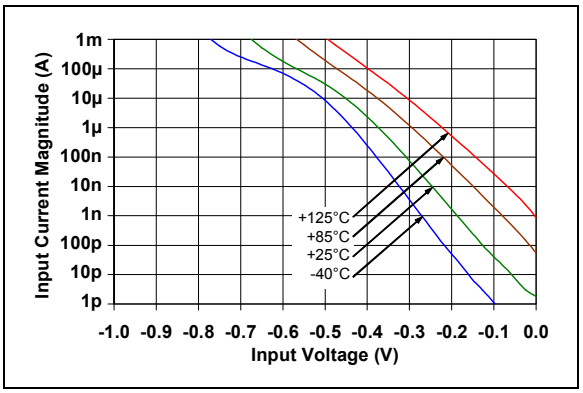

FIGURE 2-15: *Input Bias Current vs. Input Voltage (below V_{SS}).*

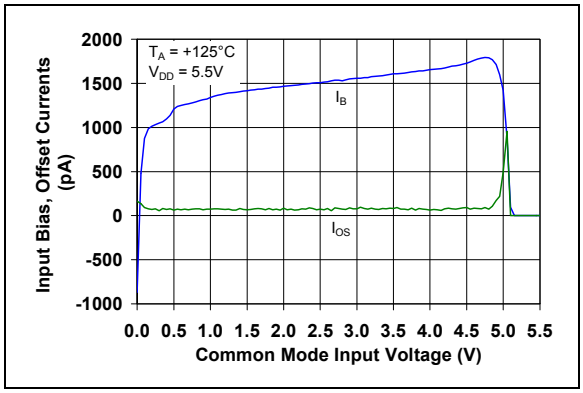

FIGURE 2-14: *Input Bias and Offset Currents vs. Common Mode Input Voltage with T_A = +125°C.*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 1 kΩ to V_L, C_L = 20 pF, and CAL/$\overline{CS}$ = V_{SS}.

2.2 Other DC Voltages and Currents

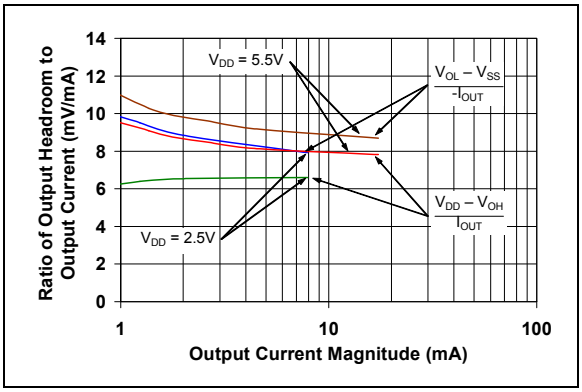

FIGURE 2-16: *Ratio of Output Voltage Headroom to Output Current.*

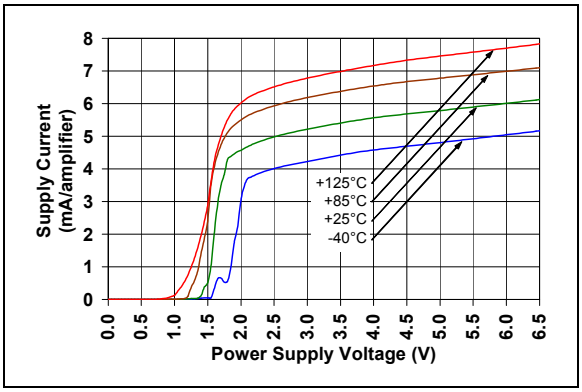

FIGURE 2-19: *Supply Current vs. Power Supply Voltage.*

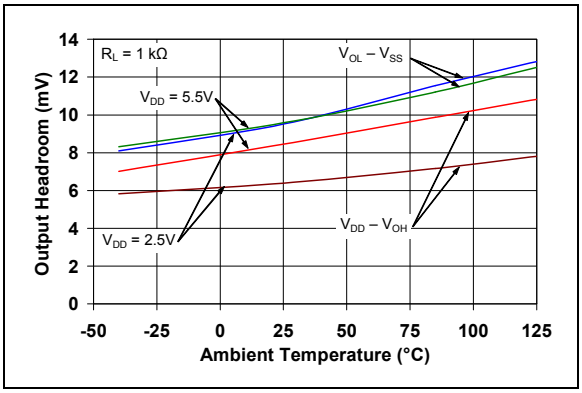

FIGURE 2-17: *Output Voltage Headroom vs. Ambient Temperature.*

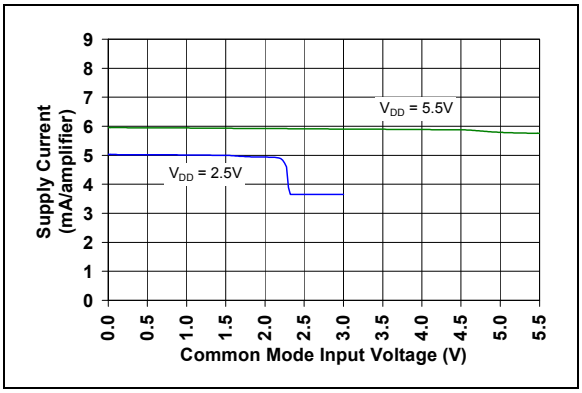

FIGURE 2-20: *Supply Current vs. Common Mode Input Voltage.*

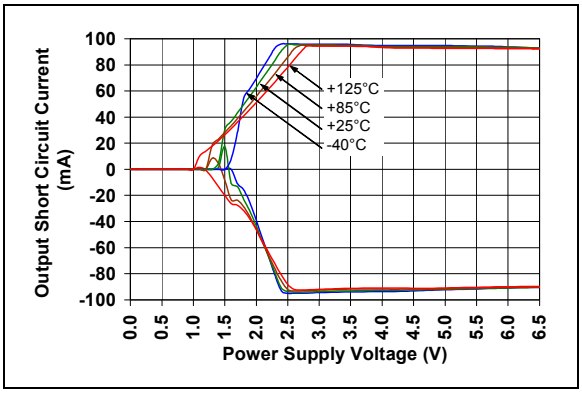

FIGURE 2-18: *Output Short-Circuit Current vs. Power Supply Voltage.*

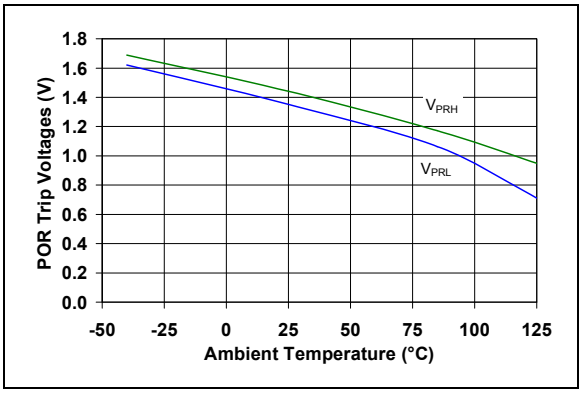

FIGURE 2-21: *Power-On Reset Voltages vs. Ambient Temperature.*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 1 kΩ to V_L, C_L = 20 pF, and CAL/$\overline{CS}$ = V_{SS}.

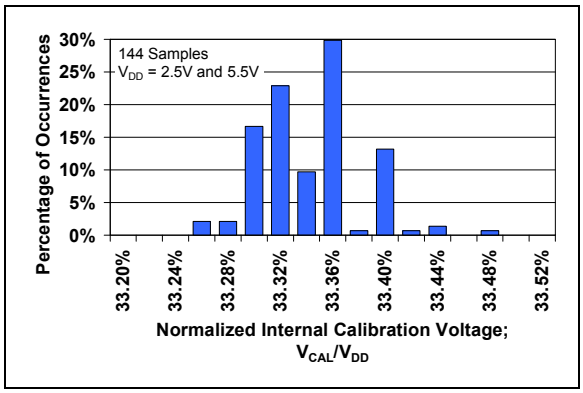

FIGURE 2-22: *Normalized Internal Calibration Voltage.*

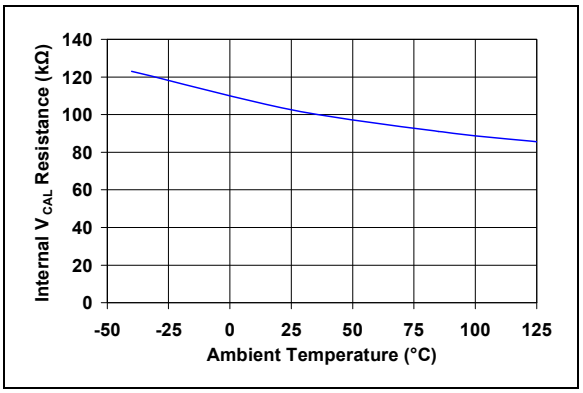

FIGURE 2-23: *V_{CAL} Input Resistance vs. Temperature.*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 1 kΩ to V_L, C_L = 20 pF, and CAL/$\overline{CS}$ = V_{SS}.

2.3 Frequency Response

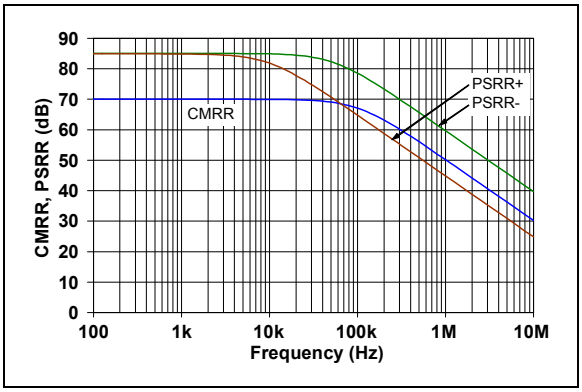

FIGURE 2-24: *CMRR and PSRR vs. Frequency.*

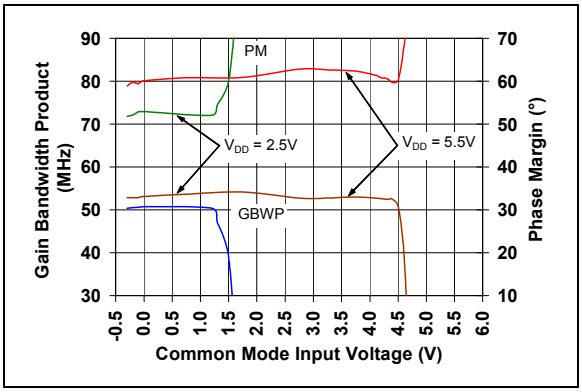

FIGURE 2-27: *Gain-Bandwidth Product and Phase Margin vs. Common Mode Input Voltage.*

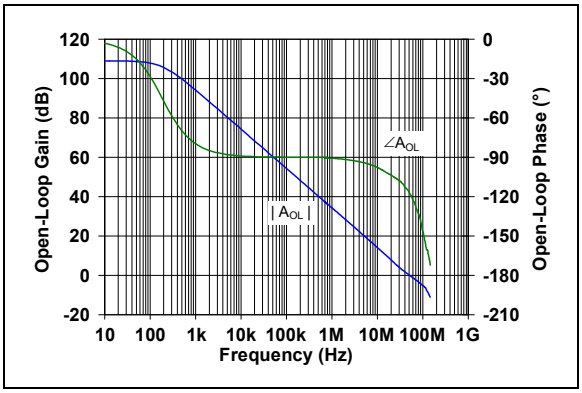

FIGURE 2-25: *Open-Loop Gain vs. Frequency.*

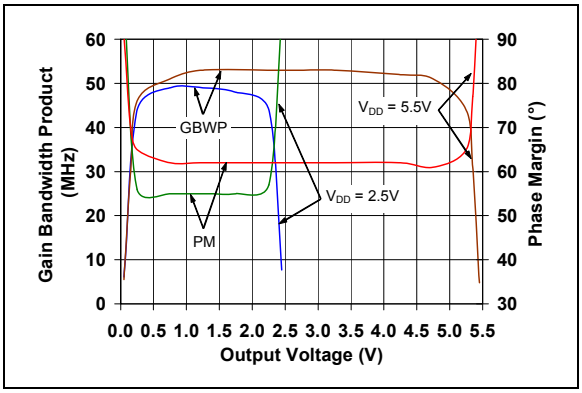

FIGURE 2-28: *Gain-Bandwidth Product and Phase Margin vs. Output Voltage.*

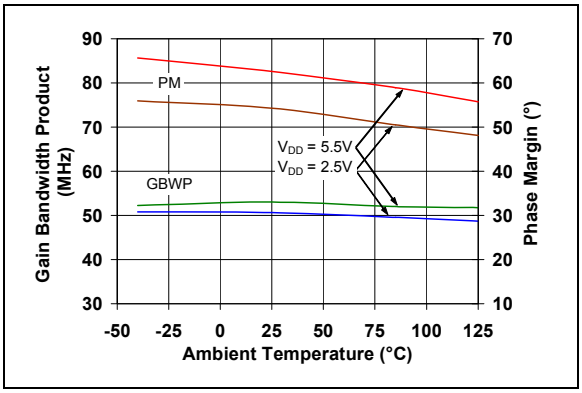

FIGURE 2-26: *Gain-Bandwidth Product and Phase Margin vs. Ambient Temperature.*

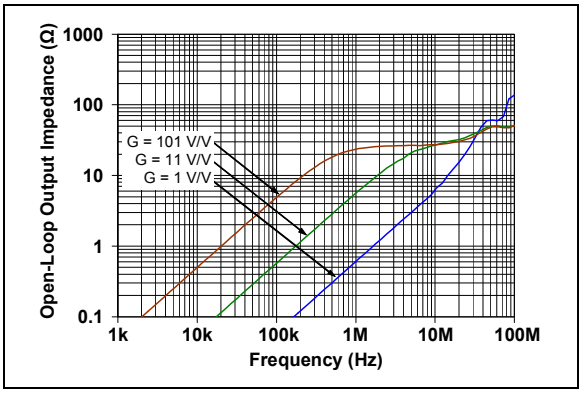

FIGURE 2-29: *Closed-Loop Output Impedance vs. Frequency.*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 1 kΩ to V_L, C_L = 20 pF, and CAL/$\overline{CS}$ = V_{SS}.

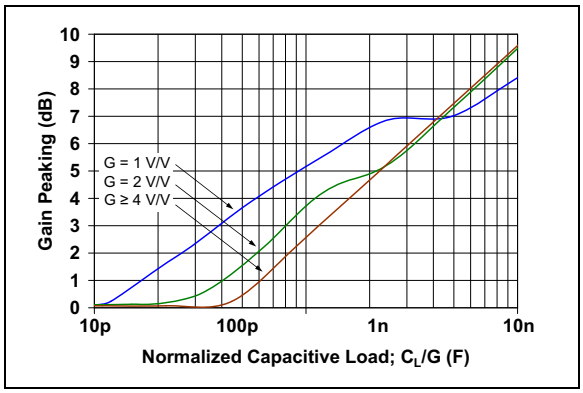

FIGURE 2-30: *Gain Peaking vs. Normalized Capacitive Load.*

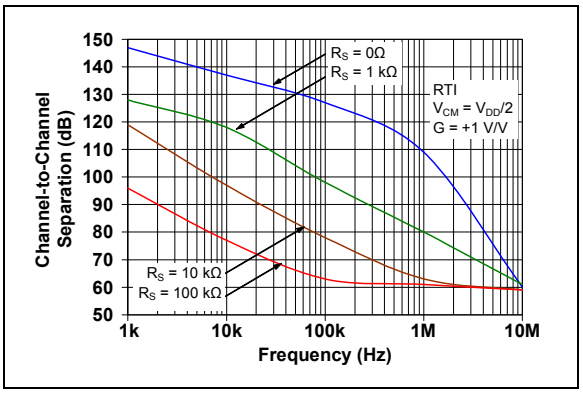

FIGURE 2-31: *Channel-to-Channel Separation vs. Frequency.*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 1 kΩ to V_L, C_L = 20 pF, and CAL/$\overline{CS}$ = V_{SS}.

2.4 Input Noise and Distortion

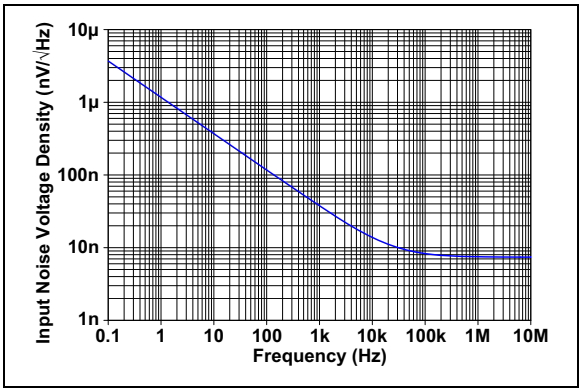

FIGURE 2-32: *Input Noise Voltage Density vs. Frequency.*

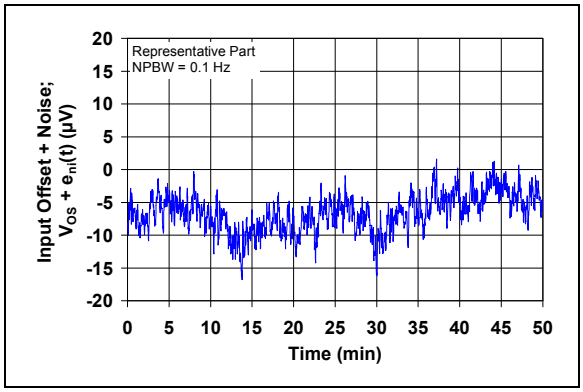

FIGURE 2-35: *Input Noise plus Offset vs. Time with 0.1 Hz Filter.*

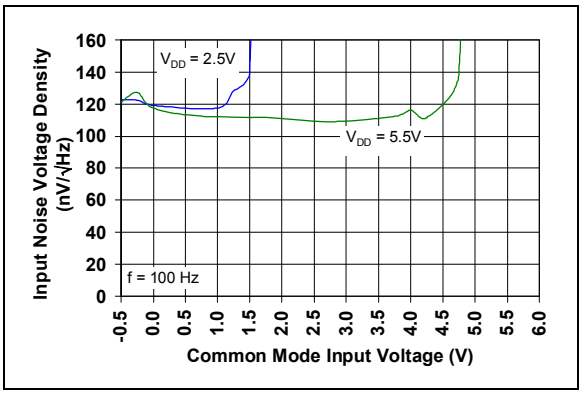

FIGURE 2-33: *Input Noise Voltage Density vs. Input Common Mode Voltage with f = 100 Hz.*

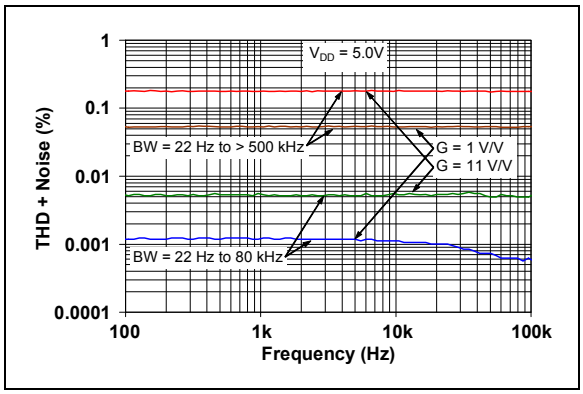

FIGURE 2-36: *THD+N vs. Frequency.*

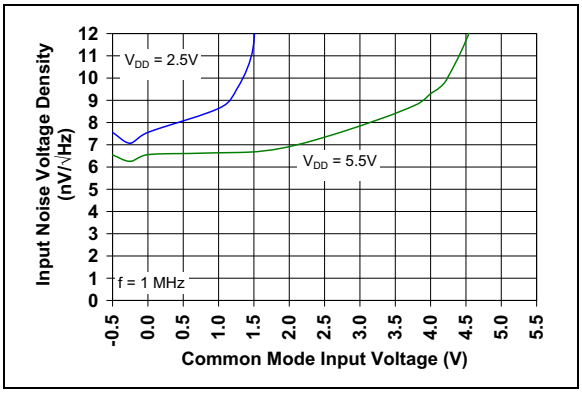

FIGURE 2-34: *Input Noise Voltage Density vs. Input Common Mode Voltage with f = 1 MHz.*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 1 kΩ to V_L, C_L = 20 pF, and CAL/$\overline{CS}$ = V_{SS}.

2.5 Time Response

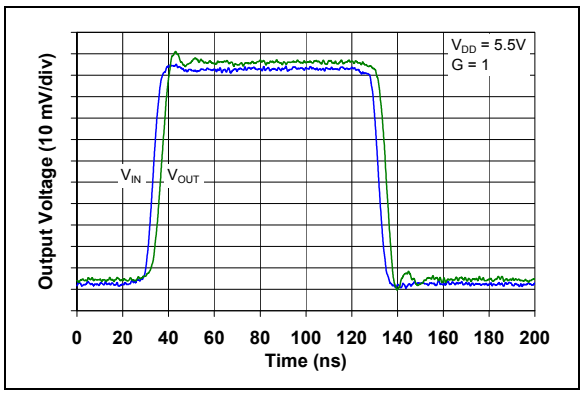

FIGURE 2-37: *Non-inverting Small Signal Step Response.*

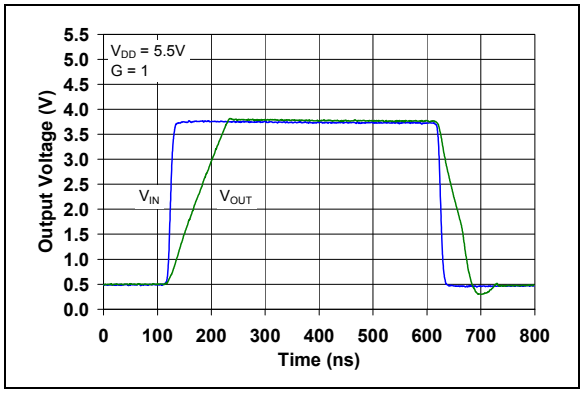

FIGURE 2-38: *Non-inverting Large Signal Step Response.*

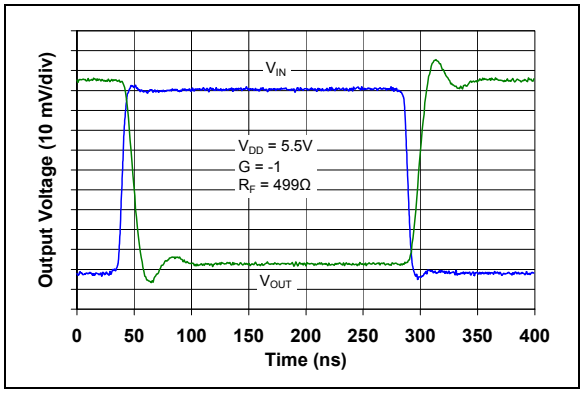

FIGURE 2-39: *Inverting Small Signal Step Response.*

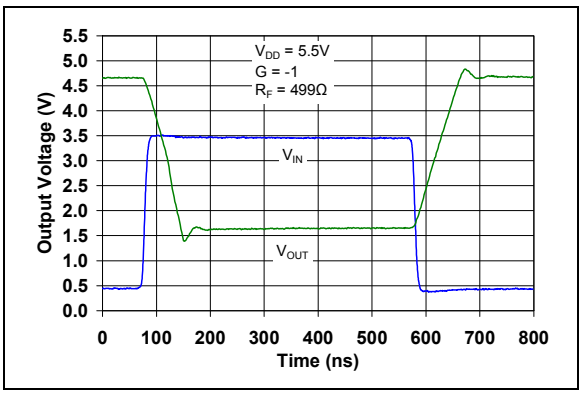

FIGURE 2-40: *Inverting Large Signal Step Response.*

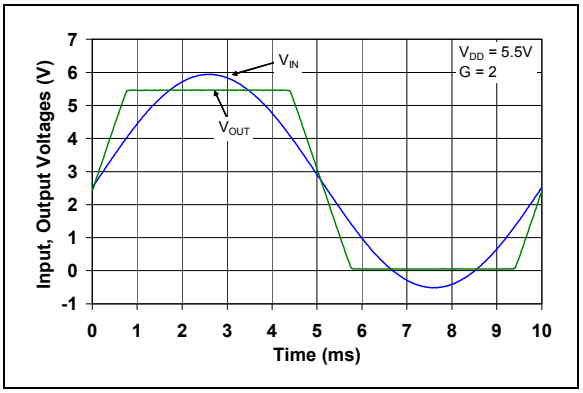

FIGURE 2-41: *The MCP651/1S/2/3/4/5/9 family shows no input phase reversal with overdrive.*

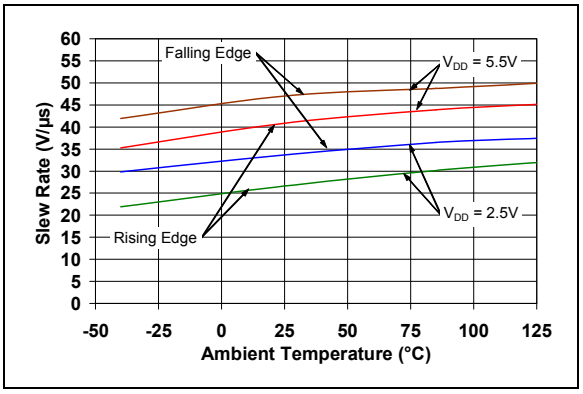

FIGURE 2-42: *Slew Rate vs. Ambient Temperature.*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 1 kΩ to V_L, C_L = 20 pF, and CAL/$\overline{CS}$ = V_{SS}.

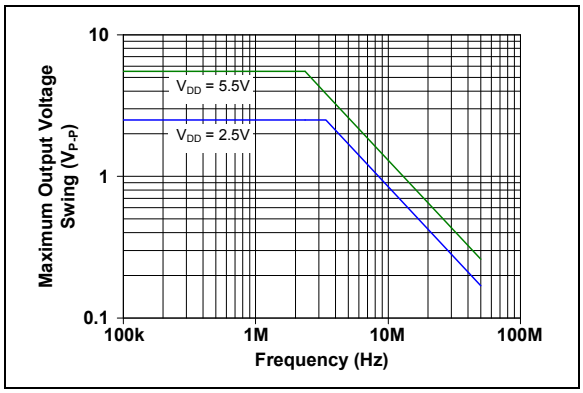

FIGURE 2-43: *Maximum Output Voltage Swing vs. Frequency.*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 1 kΩ to V_L, C_L = 20 pF, and CAL/$\overline{CS}$ = V_{SS}.

2.6 Calibration and Chip Select Response

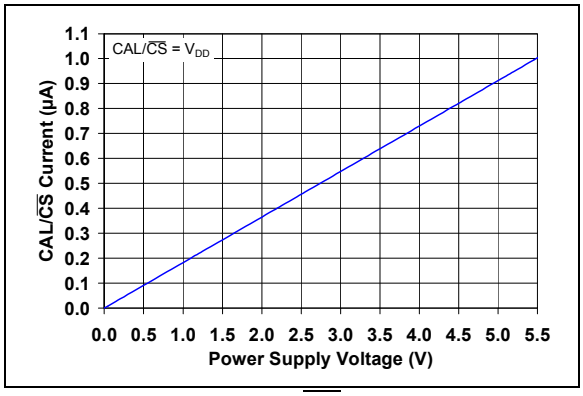

FIGURE 2-44: *CAL/$\overline{CS}$ Current vs. Power Supply Voltage.*

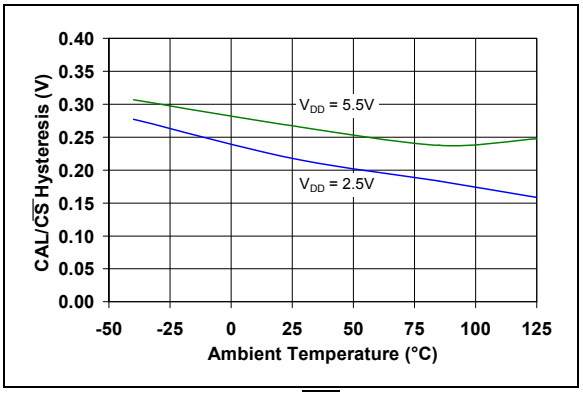

FIGURE 2-47: *CAL/$\overline{CS}$ Hysteresis vs. Ambient Temperature.*

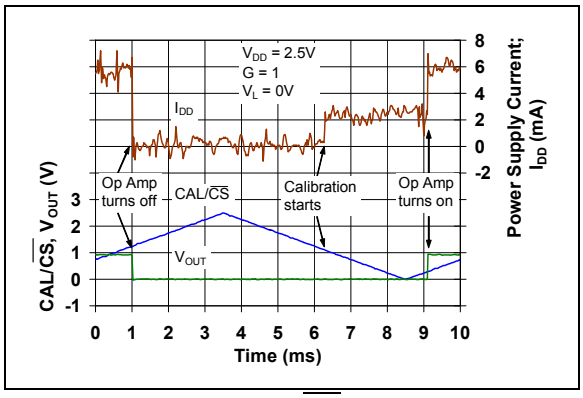

FIGURE 2-45: *CAL/$\overline{CS}$ Voltage, Output Voltage and Supply Current (for Side A) vs. Time with V_{DD} = 2.5V.*

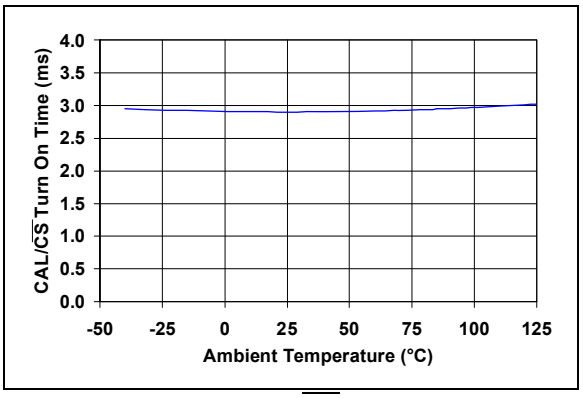

FIGURE 2-48: *CAL/$\overline{CS}$ Turn-On Time vs. Ambient Temperature.*

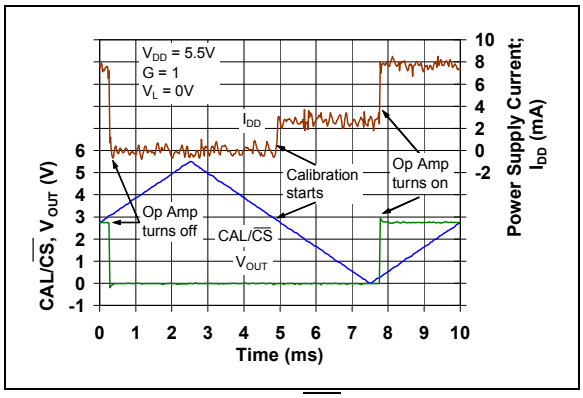

FIGURE 2-46: *CAL/$\overline{CS}$ Voltage, Output Voltage and Supply Current (for Side A) vs. Time with V_{DD} = 5.5V.*

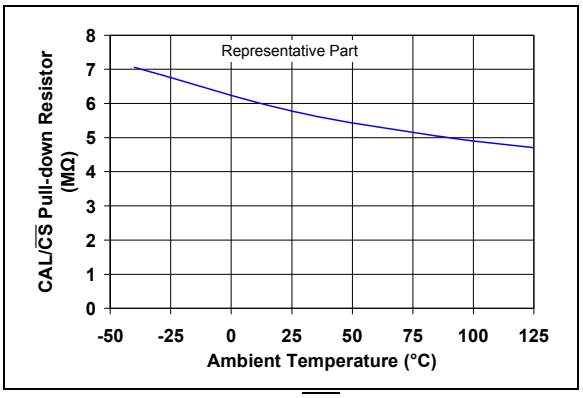

FIGURE 2-49: *CAL/$\overline{CS}$'s Pull-Down Resistor (R_{PD}) vs. Ambient Temperature.*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 1 kΩ to V_L, C_L = 20 pF, and CAL/$\overline{CS}$ = V_{SS}.

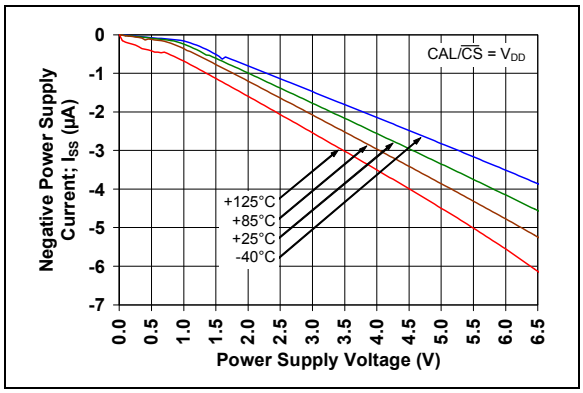

FIGURE 2-50: *Quiescent Current in Shutdown vs. Power Supply Voltage.*

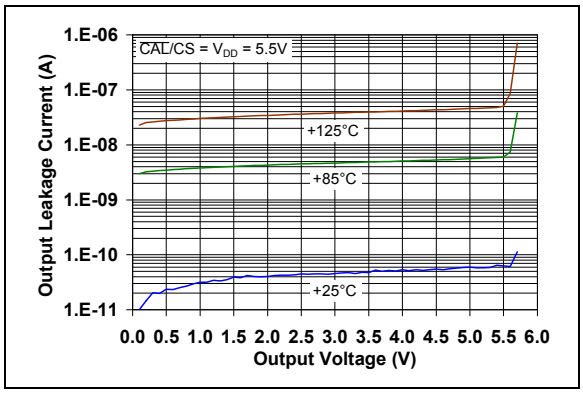

FIGURE 2-51: *Output Leakage Current vs. Output Voltage.*

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3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP651		MCP651S	MCP652		MCP653	MCP654		MCP655		MCP659	Symbol	Description
SOIC	TDFN	SOT	SOIC	DFN	SOT	SOIC	TSSOP	MSOP	DFN	QFN		
6	6	1	1	1	1	1	1	1	1	16	V_{OUT}, V_{OUTA}	Output (op amp A)
2	2	4	2	2	4	2	2	2	2	1	$V_{IN}-$, $V_{INA}-$	Inverting Input (op amp A)
3	3	3	3	3	3	3	3	3	3	2	$V_{IN}+$, $V_{INA}+$	Non-inverting Input (op amp A)
4	4	2	4	4	2	11	11	4	4	11	V_{SS}	Negative Power Supply
8	8	—	—	—	5	—	—	5	5	—	CAL/$\overline{CS}$, CAL$_A$/$\overline{CS_A}$	Calibrate/Chip Select Digital Input (op amp A)
—	—	—	—	—	—	—	—	6	6	—	CAL$_B$/$\overline{CS_B}$	Calibrate/Chip Select Digital Input (op amp B)
—	—	—	—	—	—	—	—	—	—	15	$\overline{CALAD}$/$\overline{CSAD}$	Calibrate/Chip Select Digital Input (op amps A and D)
—	—	—	—	—	—	—	—	—	—	7	$\overline{CAL_{BC}}$/$\overline{CSBC}$	Calibrate/Chip Select Digital Input (op amps B and C)
—	—	—	5	5	—	5	5	7	7	4	$V_{INB}+$	Non-inverting Input (op amp B)
—	—	—	6	6	—	6	6	8	8	5	$V_{INB}-$	Inverting Input (op amp B)
—	—	—	7	7	—	7	7	9	9	6	V_{OUTB}	Output (op amp B)
—	—	—	—	—	—	10	10	—	—	10	$V_{INC}+$	Non-inverting input (op amp C)
—	—	—	—	—	—	9	9	—	—	9	$V_{INC}-$	Inverting Input (op amp C)
—	—	—	—	—	—	8	8	—	—	8	V_{OUTC}	Output (op amp C)
—	—	—	—	—	—	12	12	—	—	12	$V_{IND}+$	Non-inverting Input (op amp D)
—	—	—	—	—	—	13	13	—	—	13	$V_{IND}-$	Inverting Input (op amp D)
—	—	—	—	—	—	14	14	—	—	14	V_{OUTD}	Output (op amp D)
7	7	5	8	8	6	4	4	10	10	3	V_{DD}	Positive Power Supply
5	5	—	—	—	—	—	—	—	—	—	V_{CAL}	Calibration Common Mode Voltage Input
1	1	—	—	—	—	—	—	—	—	—	NC	No Internal Connection
—	9	—	—	9	—	—	—	—	11	17	EP	Exposed Thermal Pad (EP); must be connected to V_{SS}

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3.1 Analog Outputs

The analog output pins (V_{OUT}) are low-impedance voltage sources.

3.2 Analog Inputs

The non-inverting and inverting inputs ($V_{IN}+$, $V_{IN}–$, …) are high-impedance CMOS inputs with low bias currents.

3.3 Power Supply Pins

The positive power supply (V_{DD}) is 2.5V to 5.5V higher than the negative power supply (V_{SS}). For normal operation, the other pins are between V_{SS} and V_{DD}.

Typically, these parts are used in a single (positive) supply configuration. In this case, V_{SS} is connected to ground and V_{DD} is connected to the supply. V_{DD} will need bypass capacitors.

3.4 Calibration Common Mode Voltage Input

A low-impedance voltage placed at this input (V_{CAL}) will set the op amps' Common mode input voltage during calibration. If this pin is left open, the Common mode input voltage during calibration is approximately $V_{DD}/3$. The internal resistor divider is disconnected from the supplies whenever the part is not in calibration.

3.5 Calibrate/Chip Select Digital Input

This input (CAL/$\overline{CS}$, …) is a CMOS, Schmitt-Triggered input that affects the Calibration and Low-Power modes of operation. When this pin goes high, the part is placed into a Low-Power mode and the output is High Z. When this pin goes low, a calibration sequence is started (which corrects V_{OS}). At the end of the calibration sequence, the output becomes low-impedance and the part resumes normal operation.

An internal POR triggers a calibration event when the part is powered on, or when the supply voltage drops too low. Thus, the MCP652 parts are calibrated, even though they do not have a CAL/$\overline{CS}$ pin.

3.6 Exposed Thermal Pad (EP)

There is an internal connection between the Exposed Thermal Pad (EP) and the V_{SS} pin; they must be connected to the same potential on the Printed Circuit Board (PCB).

This pad can be connected to a PCB ground plane to provide a larger heat sink. This improves the package thermal resistance (θ_{JA}).

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4.0 APPLICATIONS

The MCP651/1S/2/3/4/5/9 family of self-zeroed op amps is manufactured using Microchip's state-of-the-art CMOS process. It is designed for low-cost, low-power and high-precision applications. Its low supply voltage, low quiescent current and wide bandwidth makes the MCP651/1S/2/3/4/5/9 ideal for battery-powered applications.

4.1 Calibration and Chip Select

These op amps include circuitry for dynamic calibration of the offset voltage (V_{OS}).

4.1.1 mCal CALIBRATION CIRCUITRY

The internal mCal circuitry, when activated, starts a delay timer (to wait for the op amp to settle to its new bias point), then calibrates the input offset voltage (V_{OS}). The mCal circuitry is triggered at power-up (and after some power brown-out events) by the internal POR, and by the memory's Parity Detector. The power-up time, when the mCal circuitry triggers the calibration sequence, is 200 ms (typical).

4.1.2 CAL/$\overline{CS}$ PIN

The CAL/$\overline{CS}$ pin gives the user a means to externally demand a Low-Power mode of operation, then to calibrate V_{OS}. Using the CAL/$\overline{CS}$ pin makes it possible to correct V_{OS} as it drifts over time (1/f noise and aging; see Figure 2-35) and across temperature.

The CAL/$\overline{CS}$ pin performs two functions: it places the op amp(s) in a Low-Power mode when it is held high, and starts a calibration event (correction of V_{OS}) after a rising edge.

While in the Low-Power mode, the quiescent current is quite small (I_{SS} = -3 µA, typical). The output is also in a High Z state.

During the calibration event, the quiescent current is near, but smaller than, the specified quiescent current (6 mA, typical). The output continues in the High Z state, and the inputs are disconnected from the external circuit, to prevent internal signals from affecting circuit operation. The op amp inputs are internally connected to a Common mode voltage buffer and feedback resistors. The offset is corrected (using a digital state machine, logic and memory), and the calibration constants are stored in memory.

Once the calibration event is completed, the amplifier is reconnected to the external circuitry. The turn-on time, when calibration is started with the CAL/$\overline{CS}$ pin, is 3 ms (typical).

There is an internal 5 MΩ pull-down resistor tied to the CAL/$\overline{CS}$ pin. If the CAL/$\overline{CS}$ pin is left floating, the amplifier operates normally.

For the MCP655 dual and the MCP659 quad, there is an additional constraint on toggling the two CAL/$\overline{CS}$ pins close together; see the t_{CON} specification in Table 1-3. If the two pins are toggled simultaneously, or if they are toggled separately with an adequate delay between them (greater than t_{CON}), then the CAL/$\overline{CS}$ inputs are accepted as valid. If one of the two pins toggles while the other pin's calibration routine is in progress, then an invalid input occurs and the result is unpredictable.

4.1.3 INTERNAL POR

This part includes an internal Power-On Reset (POR) to protect the internal calibration memory cells. The POR monitors the power supply voltage (V_{DD}). When the POR detects a low V_{DD} event, it places the part into the Low-Power mode of operation. When the POR detects a normal V_{DD} event, it starts a delay counter, then triggers an calibration event. The additional delay gives a total POR turn-on time of 200 ms (typical); this is also the power-up time (since the POR is triggered at power-up).

4.1.4 PARITY DETECTOR

A parity error detector monitors the memory contents for any corruption. In the rare event that a parity error is detected (e.g., corruption from an alpha particle), a POR event is automatically triggered. This will cause the input offset voltage to be re-corrected, and the op amp will not return to normal operation for a period of time (the POR turn-on time, t_{PON}).

4.1.5 CALIBRATION INPUT PIN

A V_{CAL} pin is available in some options (e.g., the single MCP651) for those applications that need the calibration to occur at an internally driven Common mode voltage other than $V_{DD}/3$.

Figure 4-1 shows the reference circuit that internally sets the op amp's Common mode reference voltage (V_{CM_INT}) during calibration (the resistors are disconnected from the supplies at other times). The 5 kΩ resistor provides over-current protection for the buffer.

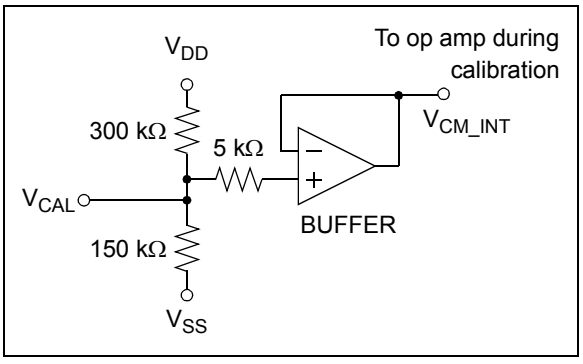

FIGURE 4-1: *Common-Mode Reference's Input Circuitry.*

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When the V_{CAL} pin is left open, the internal resistor divider generates a V_{CM_INT} of approximately $V_{DD}/3$, which is near the center of the input Common mode voltage range. It is recommended that an external capacitor from V_{CAL} to ground be added to improve noise immunity.

When the V_{CAL} pin is driven by an external voltage source, which is within its specified range, the op amp will have its input offset voltage calibrated at that Common mode input voltage. Make sure that V_{CAL} is within its specified range.

It is possible to use an external resistor voltage divider to modify V_{CM_INT}; see Figure 4-2. The internal circuitry at the V_{CAL} pin looks like 100 kΩ tied to $V_{DD}/3$. The parallel equivalent of R_1 and R_2 should be much smaller than 100 kΩ to minimize differences in matching and temperature drift between the internal and external resistors. Again, make sure that V_{CAL} is within its specified range.

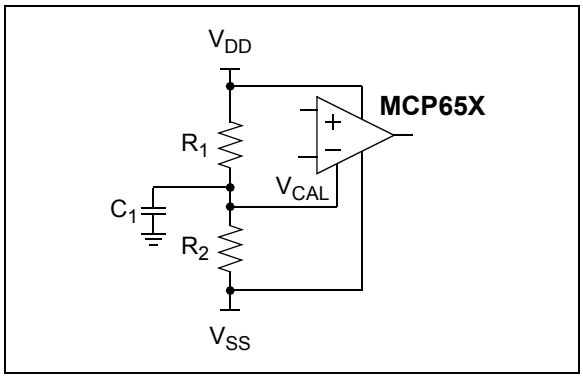

FIGURE 4-2: *Setting V_{CM} with External Resistors.*

For instance, a design goal to set V_{CM_INT} = 0.1V when V_{DD} = 2.5V could be met with: R_1 = 24.3 kΩ, R_2 = 1.00 kΩ and C_1 = 100 nF. This will keep V_{CAL} within its range for any V_{DD}, and should be close enough to 0V for ground-based applications.

4.2 Input

4.2.1 PHASE REVERSAL

The input devices are designed to not exhibit phase inversion when the input pins exceed the supply voltages. Figure 2-41 shows an input voltage exceeding both supplies with no phase inversion.

4.2.2 INPUT VOLTAGE AND CURRENT LIMITS

The ESD protection on the inputs can be depicted as shown in Figure 4-3. This structure was chosen to protect the input transistors, and to minimize input bias current (I_B). The input ESD diodes clamp the inputs when they try to go more than one diode drop below V_{SS}. They also clamp any voltages that go too far above V_{DD}; their breakdown voltage is high enough to allow normal operation, and low enough to bypass quick ESD events within the specified limits.

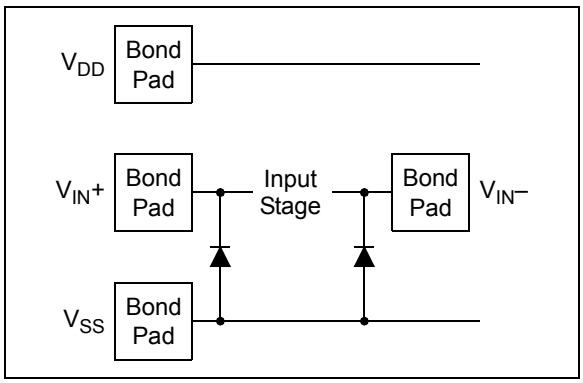

FIGURE 4-3: *Simplified Analog Input ESD Structures.*

In order to prevent damage and/or improper operation of these amplifiers, the circuit must limit the currents (and voltages) at the input pins (see **Section 1.1 "Absolute Maximum Ratings †"**). Figure 4-4 shows the recommended approach to protecting these inputs. The internal ESD diodes prevent the input pins (V_{IN}+ and V_{IN}–) from going too far below ground, and the resistors R_1 and R_2 limit the possible current drawn out of the input pins. Diodes D_1 and D_2 prevent the input pins (V_{IN}+ and V_{IN}–) from going too far above V_{DD}, and dump any currents onto V_{DD}. When implemented as shown, resistors R_1 and R_2 also limit the current through D_1 and D_2.

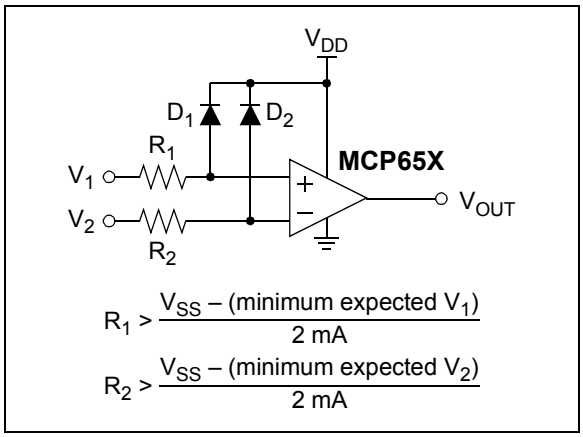

FIGURE 4-4: *Protecting the Analog Inputs.*

It is also possible to connect the diodes to the left of the resistor R_1 and R_2. In this case, the currents through the diodes D_1 and D_2 need to be limited by some other mechanism. The resistors then serve as in-rush current limiters; the DC current into the input pins (V_{IN}+ and V_{IN}–) should be very small.

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A significant amount of current can flow out of the inputs (through the ESD diodes) when the Common mode voltage (V_{CM}) is below ground (V_{SS}); see Figure 2-15. Applications that are high-impedance may need to limit the usable voltage range.

4.2.3 NORMAL OPERATION

The input stage of the MCP651/1S/2/3/4/5/9 op amps uses a differential PMOS input stage. It operates at low Common mode input voltage (V_{CM}), with V_{CM} up to V_{DD} – 1.3V and down to V_{SS} – 0.3V. The input offset voltage (V_{OS}) is measured at $V_{CM} = V_{SS} – 0.3V$ and V_{DD} – 1.3V to ensure proper operation. See Figure 2-6 and Figure 2-7 for temperature effects.

When operating at very low non-inverting gains, the output voltage is limited at the top by the V_{CM} range (< V_{DD} – 1.3V); see Figure 4-5.

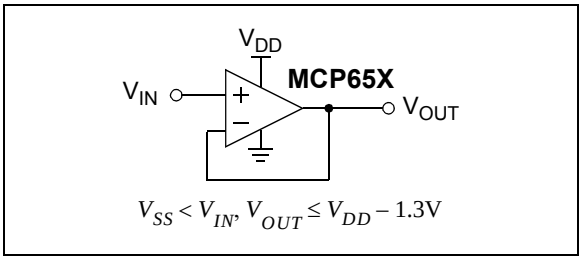

FIGURE 4-5: *Unity-Gain Voltage Limitations for Linear Operation.*

4.3 Rail-to-Rail Output

4.3.0.1 Maximum Output Voltage

The Maximum Output Voltage (see Figure 2-16 and Figure 2-17) describes the output range for a given load. For instance, the output voltage swings to within 15 mV of the negative rail with a 1 kΩ load tied to $V_{DD}/2$.

4.3.0.2 Output Current

Figure 4-6 shows the possible combinations of output voltage (V_{OUT}) and output current (I_{OUT}). I_{OUT} is positive when it flows out of the op amp into the external circuit.

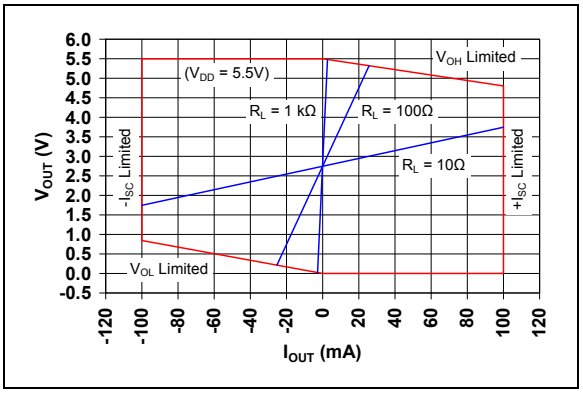

FIGURE 4-6: *Output Current.*

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4.3.0.3 Power Dissipation

Since the output short circuit current (I_{SC}) is specified at ±100 mA (typical), these op amps are capable of both delivering and dissipating significant power. Two common loads, and their impact on the op amp's power dissipation, will be discussed.

Figure 4-7 shows a resistive load (R_L) with a DC output voltage (V_{OUT}). V_L is R_L's ground point, V_{SS} is usually ground (0V) and I_{OUT} is the output current. The input currents are assumed to be negligible.

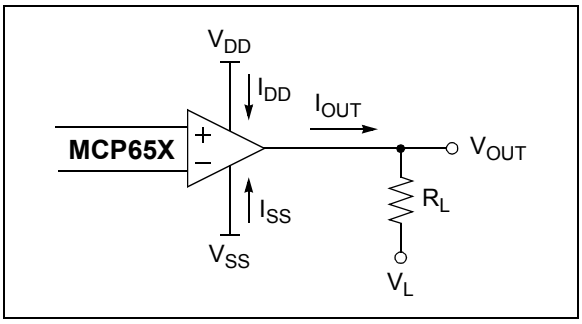

FIGURE 4-7: *Diagram for Resistive Load Power Calculations.*

The DC currents are:

EQUATION 4-1:

$$I_{OUT} = \frac{V_{OUT} - V_L}{R_L}$$

$$I_{DD} \approx I_Q + max(0, I_{OUT})$$

$$I_{SS} \approx -I_Q + min(0, I_{OUT})$$

Where:

I_Q = Quiescent supply current for one op amp (mA/amplifier)

V_{OUT} = A DC value (V)

The DC op amp power is:

EQUATION 4-2:

$$P_{OA} = I_{DD}(V_{DD} - V_{OUT}) + I_{SS}(V_{SS} - V_{OUT})$$

The maximum op amp power, for resistive loads at DC, occurs when V_{OUT} is halfway between V_{DD} and V_L or halfway between V_{SS} and V_L:

EQUATION 4-3:

$$max(P_{OA}) = I_{DD}(V_{DD} - V_{SS}) + \frac{max^2(V_{DD} - V_L, V_L - V_{SS})}{4R_L}$$

Figure 4-7 shows a capacitive load (C_L), which is driven by a sine wave with DC offset. The capacitive load causes the op amp to output higher currents at higher frequencies. Because the output rectifies I_{OUT}, the op amp's dissipated power increases (even though the capacitor does not dissipate power).

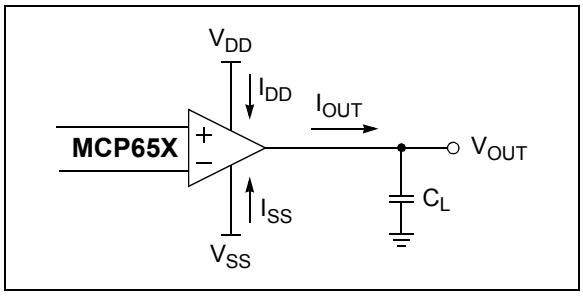

FIGURE 4-8: *Diagram for Capacitive Load Power Calculations.*

The output voltage is assumed to be:

EQUATION 4-4:

$$V_{OUT} = V_{DC} + V_{AC}sin(\omega t)$$

Where:

V_{DC} = DC offset (V)

V_{AC} = Peak output swing (V_{PK})

ω = Radian frequency ($2\pi f$) (rad/s)

The op amp's currents are:

EQUATION 4-5:

$$I_{OUT} = C_L \cdot \frac{dV_{OUT}}{dt} = V_{AC}\omega C_L cos(\omega t)$$

$$I_{DD} \approx I_Q + max(0, I_{OUT})$$

$$I_{SS} \approx -I_Q + min(0, I_{OUT})$$

Where:

I_Q = Quiescent supply current for one op amp (mA/amplifier)

The op amp's instantaneous power, average power and peak power are:

EQUATION 4-6:

$$P_{OA} = I_{DD}(V_{DD} - V_{OUT}) + I_{SS}(V_{SS} - V_{OUT})$$

$$ave(P_{OA}) = (V_{DD} - V_{SS})\left(I_Q + \frac{4V_{AC}fC_L}{\pi}\right)$$

$$max(P_{OA}) = (V_{DD} - V_{SS})(I_Q + 2V_{AC}fC_L)$$

The power dissipated in a package depends on the powers dissipated by each op amp in that package:

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EQUATION 4-7:

$$P_{PKG} = \sum_{k=1}^{n} P_{OA}$$

Where:

n = Number of op amps in package (1 or 2)

The maximum ambient to junction temperature rise (ΔT_{JA}) and junction temperature (T_J) can be calculated using the maximum expected package power (P_{PKG}), ambient temperature (T_A) and the package thermal resistance (θ_{JA}) found in Table 1-4:

EQUATION 4-8:

$$\Delta T_{JA} = P_{PKG}\theta_{JA}$$
$$T_J = T_A + \Delta T_{JA}$$

The worst-case power de-rating for the op amps in a particular package can be easily calculated:

EQUATION 4-9:

$$P_{PKG} \leq \frac{T_{Jmax} - T_A}{\theta_{JA}}$$

Where:

T_{Jmax} = Absolute maximum junction temperature (°C)

T_A = Ambient temperature (°C)

Several techniques are available to reduce ΔT_{JA} for a given package:

- Reduce θ_{JA}
  - Use another package
  - Improve the PCB layout (ground plane, etc.)
  - Add heat sinks and air flow
- Reduce *max*(P_{PKG})
  - Increase R_L
  - Decrease C_L
  - Limit I_{OUT} using R_{ISO} (see Figure 4-9)
  - Decrease V_{DD}

4.4 Improving Stability

4.4.1 CAPACITIVE LOADS

Driving large capacitive loads can cause stability problems for voltage feedback op amps. As the load capacitance increases, the feedback loop's phase margin decreases and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in the step response. See Figure 2-30. A unity-gain buffer (G = +1) is the most sensitive to capacitive loads, though all gains show the same general behavior.

When driving large capacitive loads with these op amps (e.g., > 20 pF when G = +1), a small series resistor at the output (R_{ISO} in Figure 4-9) improves the feedback loop's phase margin (stability) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitive load.

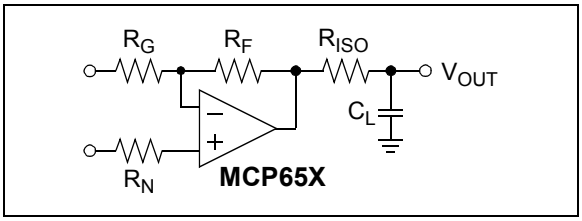

FIGURE 4-9: *Output Resistor, R_{ISO} Stabilizes Large Capacitive Loads.*

Figure 4-10 gives recommended R_{ISO} values for different capacitive loads and gains. The x-axis is the normalized load capacitance (C_L/G_N), where G_N is the circuit's noise gain. For non-inverting gains, G_N and the Signal Gain are equal. For inverting gains, G_N is 1+|Signal Gain| (e.g., -1 V/V gives G_N = +2 V/V).

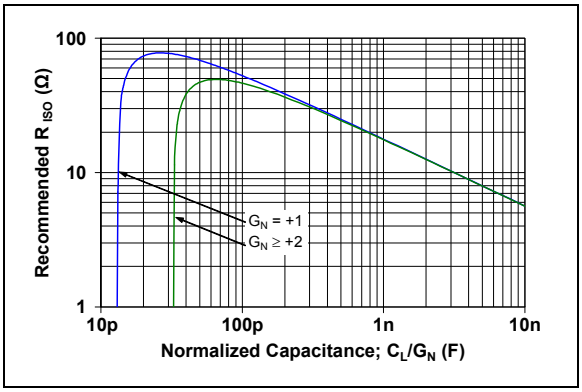

FIGURE 4-10: *Recommended R_{ISO} Values for Capacitive Loads.*

After selecting R_{ISO} for your circuit, double check the resulting frequency response peaking and step response overshoot. Modify R_{ISO}'s value until the response is reasonable. Bench evaluation and simulations with the MCP651/1S/2/3/4/5/9 SPICE macro model are helpful.

4.4.2 GAIN PEAKING

Figure 4-11 shows an op amp circuit that represents non-inverting amplifiers (V_M is a DC voltage and V_P is the input) or inverting amplifiers (V_P is a DC voltage and V_M is the input). The capacitances C_N and C_G represent the total capacitance at the input pins; they include the op amp's Common mode input capacitance (C_{CM}), board parasitic capacitance and any capacitor placed in parallel.

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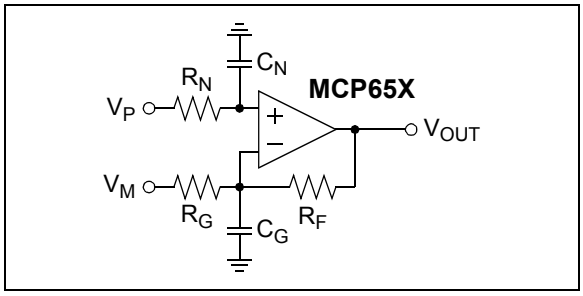

FIGURE 4-11: *Amplifier with Parasitic Capacitance.*

C_G acts in parallel with R_G (except for a gain of +1 V/V), which causes an increase in gain at high frequencies. C_G also reduces the phase margin of the feedback loop, which becomes less stable. This effect can be reduced by either reducing C_G or R_F.

C_N and R_N form a low-pass filter that affects the signal at V_P. This filter has a single real pole at $1/(2\pi R_N C_N)$.

The largest value of R_F that should be used depends on noise gain (see G_N in **Section 4.4.1 "Capacitive Loads"**) and C_G. Figure 4-12 shows the maximum recommended R_F for several C_G values.

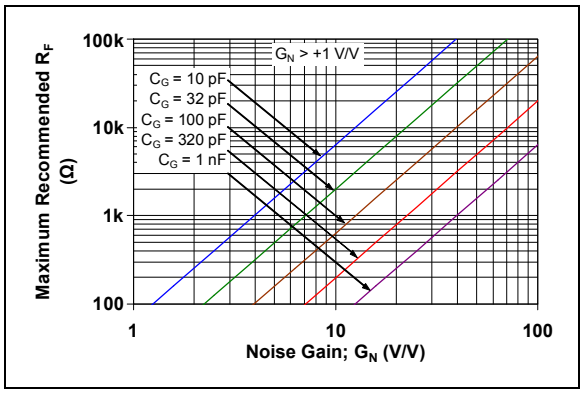

FIGURE 4-12: *Maximum Recommended R_F vs. Gain.*

Figure 2-37 and Figure 2-38 show the small signal and large signal step responses at G = +1 V/V. The unity-gain buffer usually has R_F = 0Ω and R_G open.

Figure 2-39 and Figure 2-40 show the small signal and large signal step responses at G = -1 V/V. Since the noise gain is 2 V/V and $C_G \approx$ 10 pF, the resistors were chosen to be $R_F = R_G$ = 499Ω and R_N = 249Ω.

It is also possible to add a capacitor (C_F) in parallel with R_F to compensate for the de-stabilizing effect of C_G. This makes it possible to use larger values of R_F. The conditions for stability are summarized in Equation 4-10.

EQUATION 4-10:

Given:

$$G_{N1} = 1 + R_F/R_G$$
$$G_{N2} = 1 + C_G/C_F$$
$$f_F = 1/(2\pi R_F C_F)$$
$$f_Z = f_F(G_{N1}/G_{N2})$$

We need:

$$f_F \leq f_{GBWP}/(2G_{N2}), \quad G_{N1} < G_{N2}$$
$$f_F \leq f_{GBWP}/(4G_{N1}), \quad G_{N1} > G_{N2}$$

4.5 Power Supply

With this family of operational amplifiers, the Power Supply pin (V_{DD} for single supply) should have a local bypass capacitor (i.e., 0.01 µF to 0.1 µF) within 2 mm for good high-frequency performance. Surface mount, multilayer ceramic capacitors, or their equivalent, should be used.

These op amps require a bulk capacitor (i.e., 2.2 µF or larger) within 50 mm to provide large, slow currents. Tantalum capacitors, or their equivalent, may be a good choice. This bulk capacitor can be shared with other nearby analog parts as long as crosstalk through the supplies does not prove to be a problem.

4.6 High-Speed PCB Layout

These op amps are fast enough that a little extra care in the PCB (Printed Circuit Board) layout can make a significant difference in performance. Good PCB layout techniques will help achieve the performance shown in the specifications and Typical Performance Curves; it will also help minimize EMC (Electro-Magnetic Compatibility) issues.

Use a solid ground plane. Connect the bypass local capacitor(s) to this plane with minimal length traces to cut down inductive and capacitive crosstalk.

Separate digital from analog, low-speed from high-speed, and low-power from high-power. This will reduce interference.

Keep sensitive traces short and straight. Separate them from interfering components and traces. This is especially important for high-frequency (low rise time) signals.

Sometimes, it helps to place guard traces next to victim traces. They should be on both sides of the victim trace, and as close as possible. Connect guard traces to ground plane at both ends, and in the middle for long traces.

Use coax cables, or low inductance wiring, to route signal and power to and from the PCB. Mutual and self inductance of power wires is often a cause of crosstalk and unusual behavior.

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4.7 Typical Applications

4.7.1 POWER DRIVER WITH HIGH GAIN

Figure 4-13 shows a power driver with high gain ($1 + R_2/R_1$). The MCP651/1S/2/3/4/5/9 op amp's short-circuit current makes it possible to drive significant loads. The calibrated input offset voltage supports accurate response at high gains. R_3 should be small, and equal to $R_1||R_2$, in order to minimize the bias current induced offset.

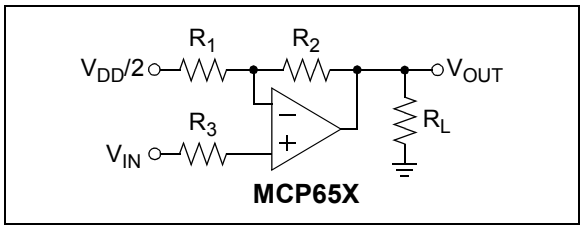

FIGURE 4-13: *Power Driver.*

4.7.2 OPTICAL DETECTOR AMPLIFIER

Figure 4-14 shows a transimpedance amplifier, using the MCP651 op amp, in a photo detector circuit. The photo detector is a capacitive current source. The op amp's input Common mode capacitance (5 pF, typical) acts in parallel with C_D. R_F provides enough gain to produce 10 mV at V_{OUT}. C_F stabilizes the gain and limits the transimpedance bandwidth to about 1.1 MHz. R_F's parasitic capacitance (e.g., 0.2 pF for a 0805 SMD) acts in parallel with C_F.

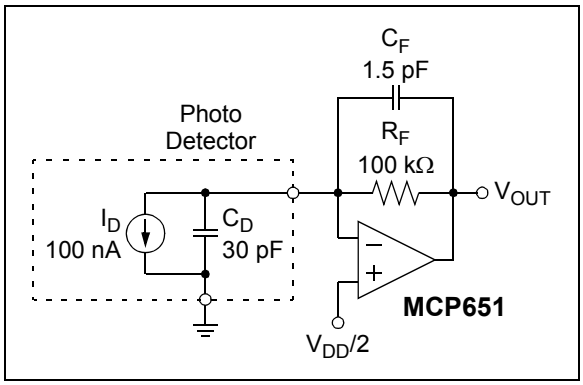

FIGURE 4-14: *Transimpedance Amplifier for an Optical Detector.*

4.7.3 H-BRIDGE DRIVER

Figure 4-15 shows the MCP652 dual op amp used as a H-bridge driver. The load could be a speaker or a DC motor.

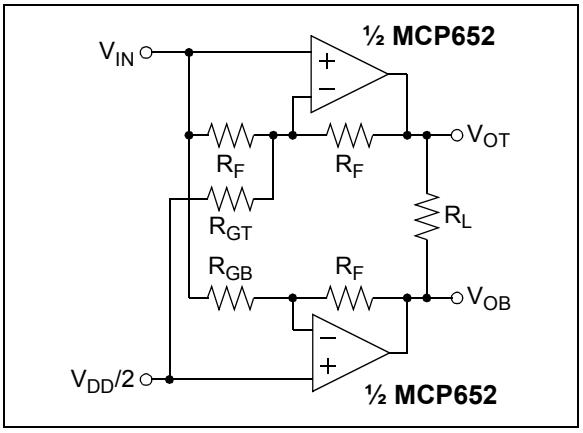

FIGURE 4-15: *H-Bridge Driver.*

This circuit automatically makes the noise gains (G_N) equal, when the gains are set properly, so that the frequency responses match well (in magnitude and in phase). Equation 4-11 shows how to calculate R_{GT} and R_{GB} so that both op amps have the same DC gains; G_{DM} needs to be selected first.

EQUATION 4-11:

$$G_{DM} \equiv \frac{V_{OT} - V_{OB}}{V_{IN} - V_{DD}/2} \geq 2\ V/V$$

$$R_{GT} = \frac{R_F}{(G_{DM}/2) - 1}$$

$$R_{GB} = \frac{R_F}{G_{DM}/2}$$

Equation 4-12 gives the resulting Common mode and Differential mode output voltages.

EQUATION 4-12:

$$\frac{V_{OT} + V_{OB}}{2} = \frac{V_{DD}}{2}$$

$$V_{OT} - V_{OB} = G_{DM}\left(V_{IN} - \frac{V_{DD}}{2}\right)$$

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5.0 DESIGN AIDS

Microchip provides the basic design aids needed for the MCP651/1S/2/3/4/5/9 family of op amps.

5.1 SPICE Macro Model

The latest SPICE macro model for the MCP651/1S/2/3/4/5/9 op amps is available on the Microchip web site at www.microchip.com. This model is intended to be an initial design tool that works well in the op amp's linear region of operation over the temperature range. See the model file for information on its capabilities.

Bench testing is a very important part of any design and cannot be replaced with simulations. Also, simulation results using this macro model need to be validated by comparing them to the data sheet specifications and characteristic curves.

5.2 FilterLab® Software

Microchip's FilterLab® software is an innovative software tool that simplifies analog active filter (using op amps) design. Available at no cost from the Microchip web site at www.microchip.com/filterlab, the FilterLab design tool provides full schematic diagrams of the filter circuit with component values. It also outputs the filter circuit in SPICE format, which can be used with the macro model to simulate actual filter performance.

5.3 Microchip Advanced Part Selector (MAPS)

MAPS is a software tool that helps efficiently identify Microchip devices that fit a particular design requirement. Available at no cost from the Microchip web site at www.microchip.com/maps, the MAPS is an overall selection tool for Microchip's product portfolio that includes Analog, Memory, MCUs and DSCs. Using this tool, a customer can define a filter to sort features for a parametric search of devices and export side-by-side technical comparison reports. Helpful links are also provided for data sheets, purchase and sampling of Microchip parts.

5.4 Analog Demonstration and Evaluation Boards

Microchip offers a broad spectrum of Analog Demonstration and Evaluation Boards that are designed to help customers achieve faster time to market. For a complete listing of these boards and their corresponding user's guides and technical information, visit the Microchip web site at www.microchip.com/analog tools.

Some boards that are especially useful are:

- MCP6XXX Amplifier Evaluation Board 1
- MCP6XXX Amplifier Evaluation Board 2
- MCP6XXX Amplifier Evaluation Board 3
- MCP6XXX Amplifier Evaluation Board 4
- Active Filter Demo Board Kit
- 8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board, P/N SOIC8EV

5.5 Application Notes

The following Microchip Application Notes are available on the Microchip web site at www.microchip.com/appnotes and are recommended as supplemental reference resources.

- **ADN003:** *"Select the Right Operational Amplifier for your Filtering Circuits"* (DS21821)
- **AN722:** *"Operational Amplifier Topologies and DC Specifications"* (DS00722)
- **AN723:** *"Operational Amplifier AC Specifications and Applications"* (DS00723)
- **AN884:** *"Driving Capacitive Loads With Op Amps"* (DS00884)
- **AN990:** *"Analog Sensor Conditioning Circuits – An Overview"* (DS00990)
- **AN1177:** *"Op Amp Precision Design: DC Errors"* (DS01177)
- **AN1228:** *"Op Amp Precision Design: Random Noise"* (DS01228)
- **AN1332:** *"Current Sensing Circuit Concepts and Fundamentals" (*DS01332)

Some of these application notes, and others, are listed in the design guide:

- "Signal Chain Design Guide" (DS21825)

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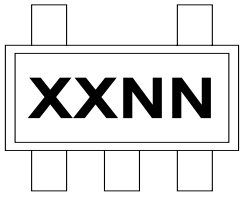
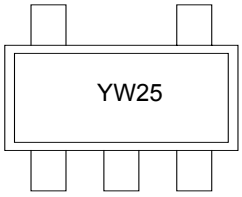
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

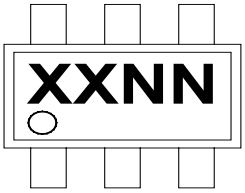
5-Lead SOT-23 (2x3) **(MCP651S)**



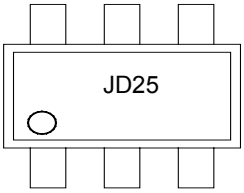
Example:



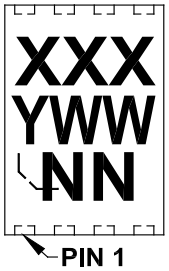
6-Lead SOT-23 (2x3) **(MCP653)**



Example:



8-Lead TDFN(2x3) **(MCP651)**



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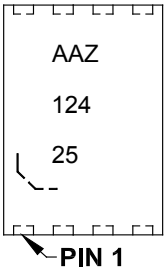
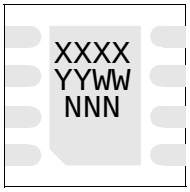


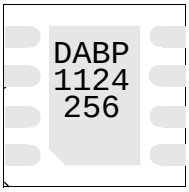
8-Lead DFN (3x3) **(MCP652)**



Device	Code
MCP652	DABP

Note: Applies to 8-Lead 3x3 DFN

Example:



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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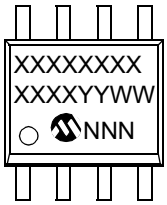
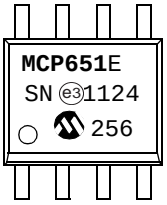
6.2 Package Marking Information

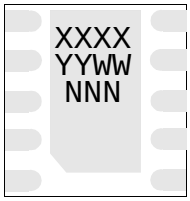
8-Lead SOIC (150 mil) **(MCP651, MCP652)**



Example:



10-Lead DFN (3x3) **(MCP655)**



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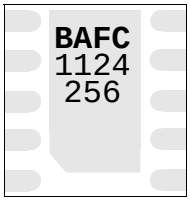
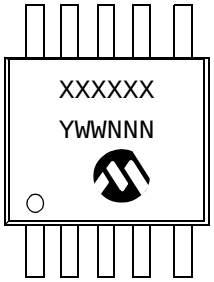


10-Lead MSOP **(MCP655)**

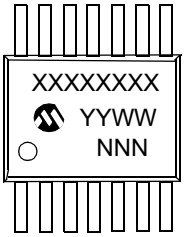


Example:

14-Lead SOIC **(MCP654)**

Example:

14-Lead TSSOP **(MCP654)**



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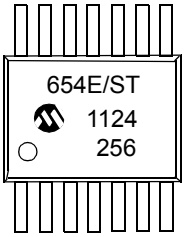
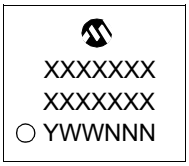


16-Lead QFN (4x4) **(MCP659)**



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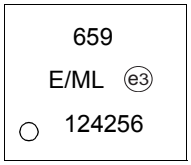

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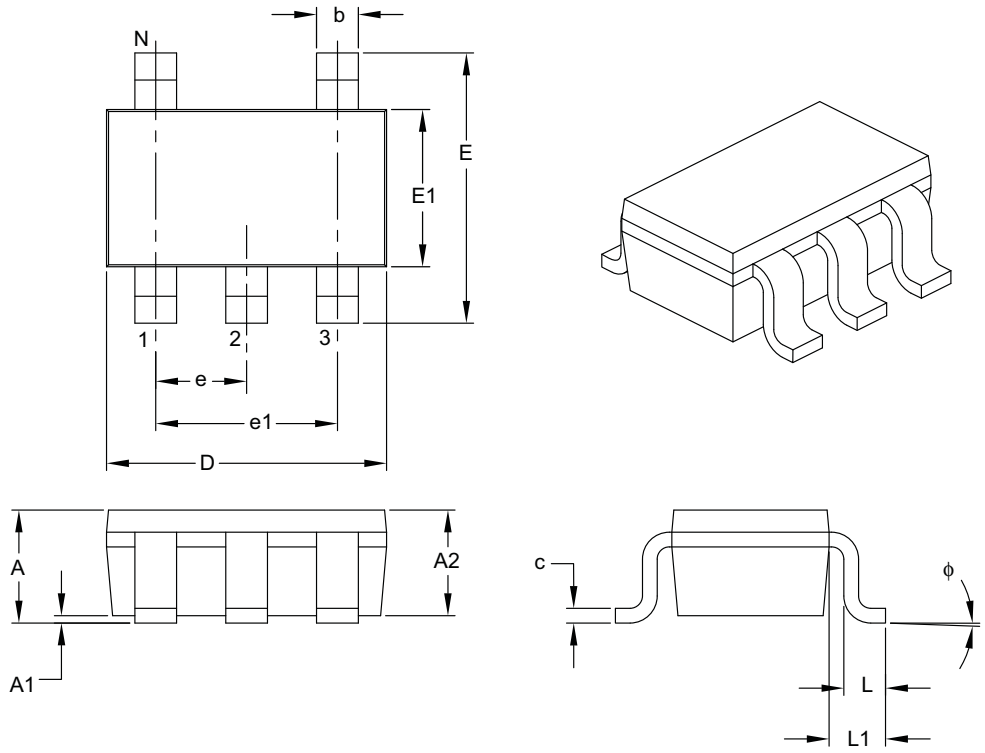
5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		5	
Lead Pitch	e		0.95 BSC	
Outside Lead Pitch	e1		1.90 BSC	
Overall Height	A	0.90	–	1.45
Molded Package Thickness	A2	0.89	–	1.30
Standoff	A1	0.00	–	0.15
Overall Width	E	2.20	–	3.20
Molded Package Width	E1	1.30	–	1.80
Overall Length	D	2.70	–	3.10
Foot Length	L	0.10	–	0.60
Footprint	L1	0.35	–	0.80
Foot Angle	ϕ	0°	–	30°
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.20	–	0.51

Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-091B

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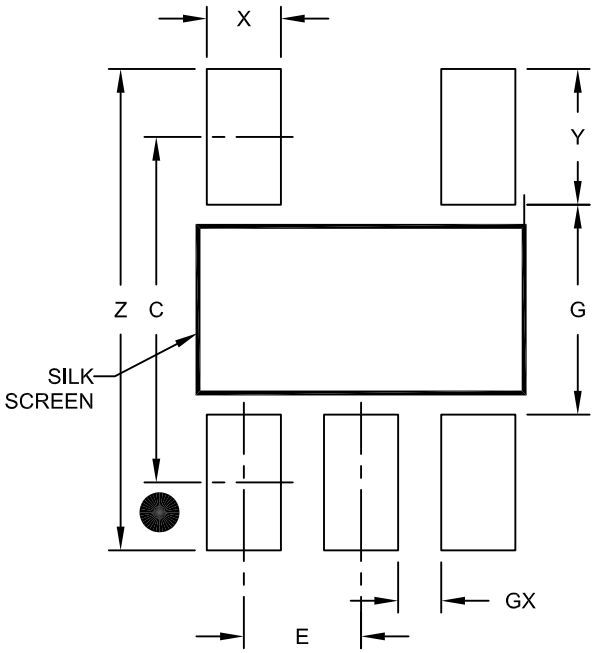
5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.95 BSC	
Contact Pad Spacing	C		2.80	
Contact Pad Width (X5)	X			0.60
Contact Pad Length (X5)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2091A

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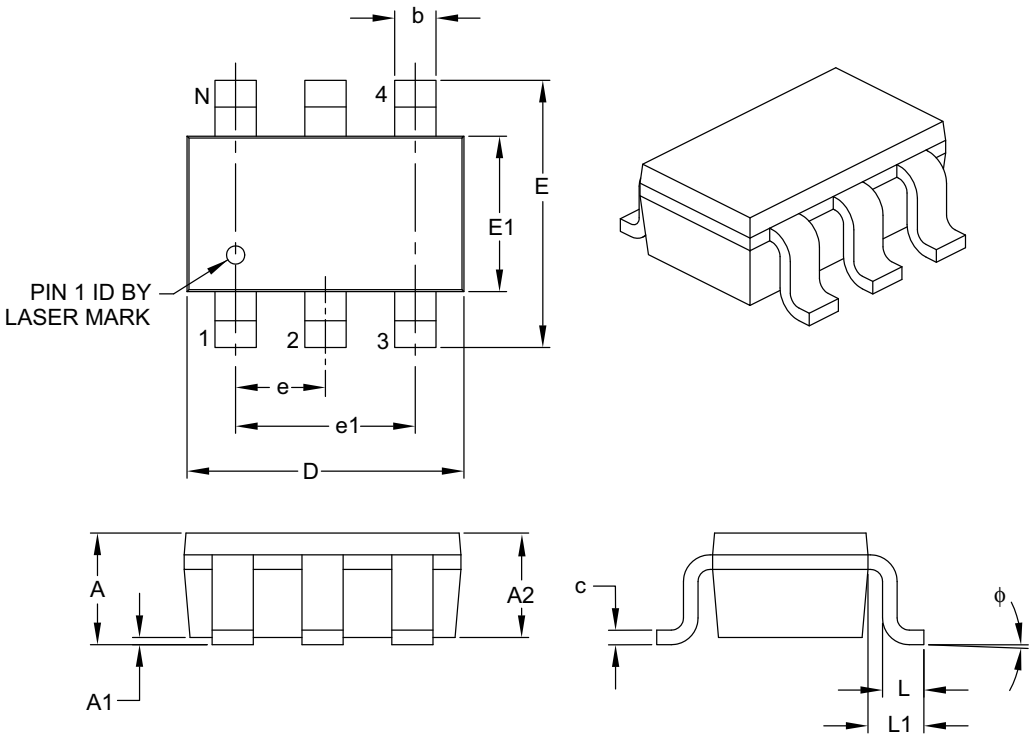
6-Lead Plastic Small Outline Transistor (CHY) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		6	
Pitch	e		0.95 BSC	
Outside Lead Pitch	e1		1.90 BSC	
Overall Height	A	0.90	–	1.45
Molded Package Thickness	A2	0.89	–	1.30
Standoff	A1	0.00	–	0.15
Overall Width	E	2.20	–	3.20
Molded Package Width	E1	1.30	–	1.80
Overall Length	D	2.70	–	3.10
Foot Length	L	0.10	–	0.60
Footprint	L1	0.35	–	0.80
Foot Angle	ϕ	0°	–	30°
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.20	–	0.51

Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-028B

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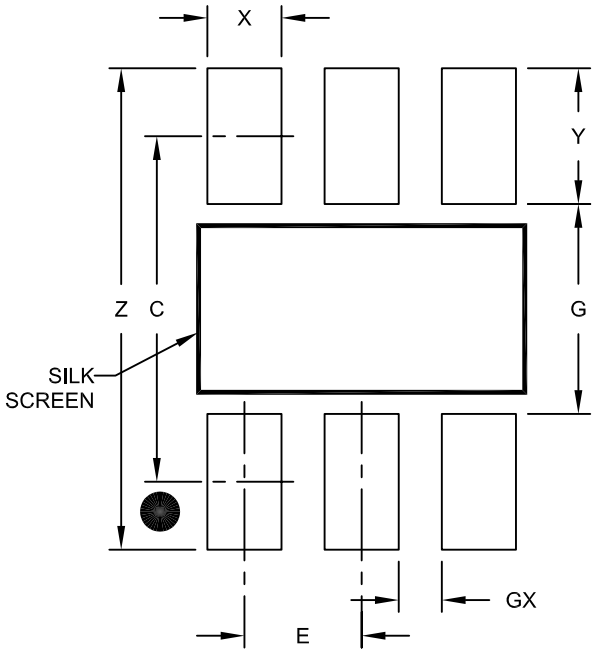
6-Lead Plastic Small Outline Transistor (CHY) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.95 BSC	
Contact Pad Spacing	C		2.80	
Contact Pad Width (X6)	X			0.60
Contact Pad Length (X6)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2028A

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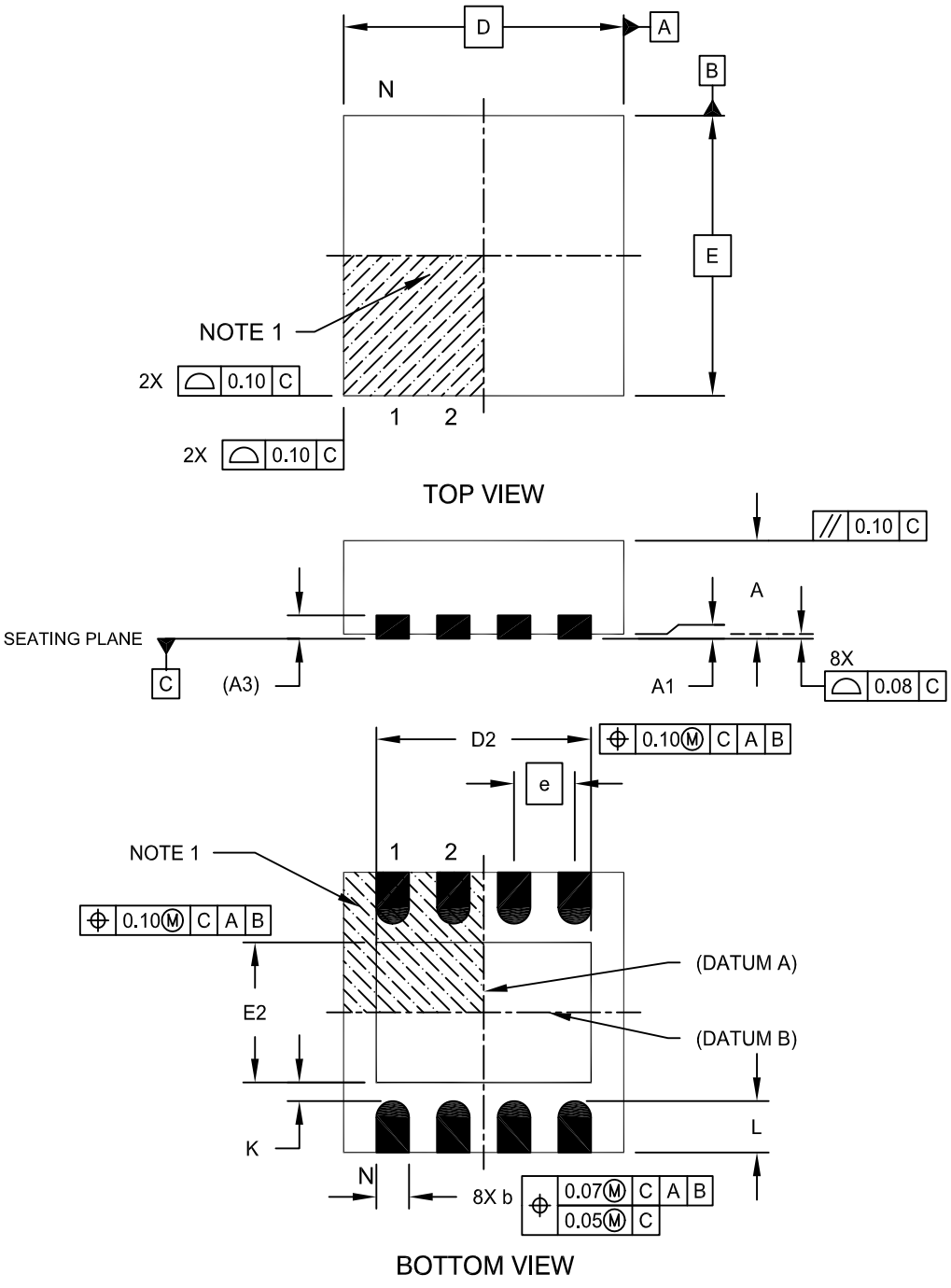
8-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-062C Sheet 1 of 2

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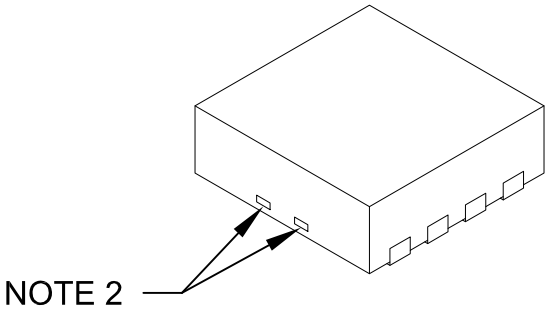
8-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		3.00 BSC	
Exposed Pad Width	E2	1.34	-	1.60
Overall Width	E		3.00 BSC	
Exposed Pad Length	D2	1.60	-	2.40
Contact Width	b	0.25	0.30	0.35
Contact Length	L	0.20	0.30	0.55
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-062C Sheet 2 of 2

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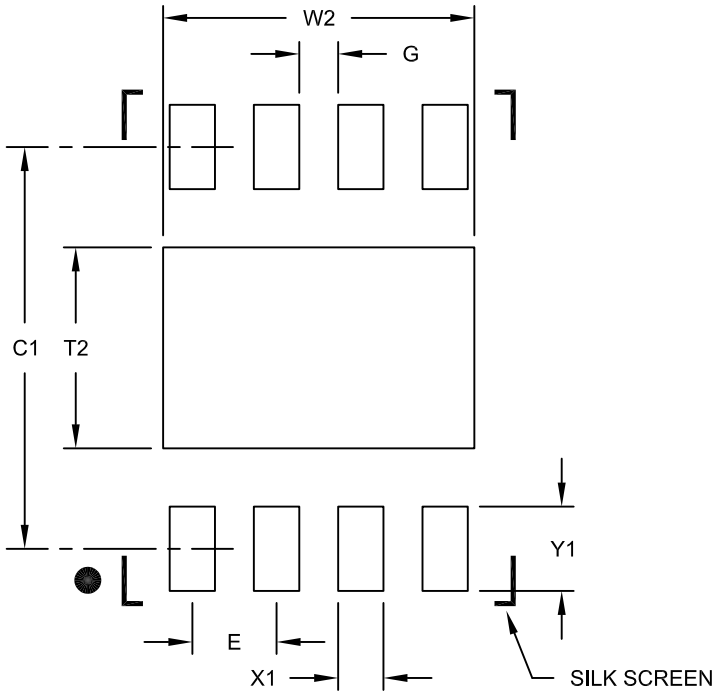
8-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	W2			2.40
Optional Center Pad Length	T2			1.55
Contact Pad Spacing	C1		3.10	
Contact Pad Width (X8)	X1			0.35
Contact Pad Length (X8)	Y1			0.65
Distance Between Pads	G	0.30		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2062B

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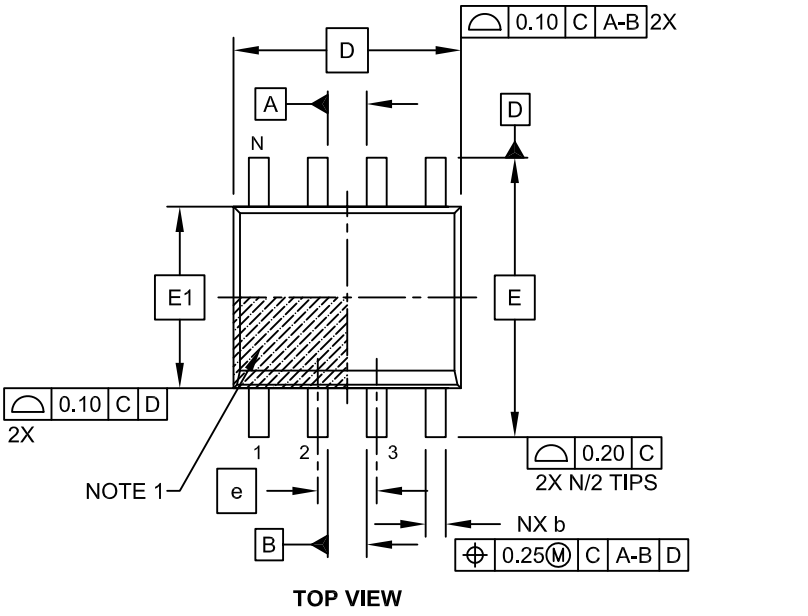
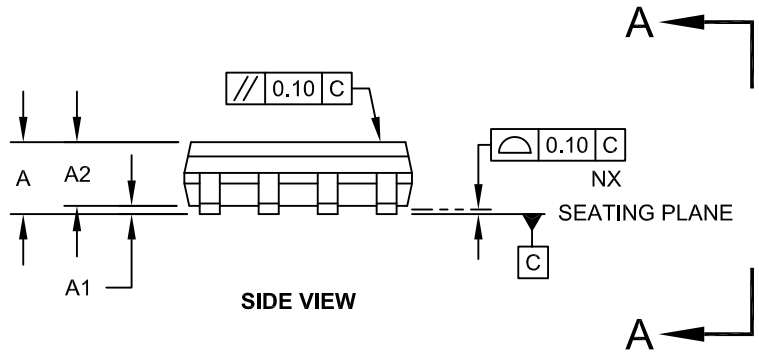
8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

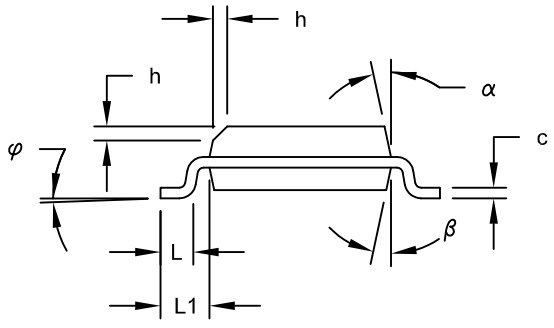
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW



VIEW A-A

Microchip Technology Drawing No. C04-057C Sheet 1 of 2

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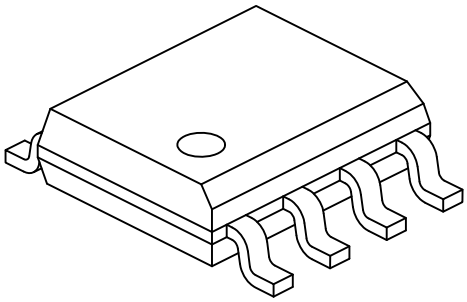
8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2

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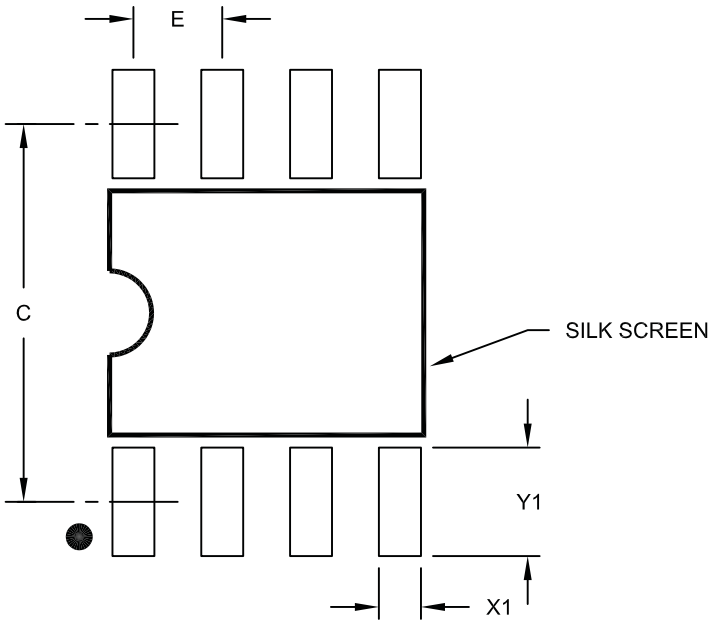
8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

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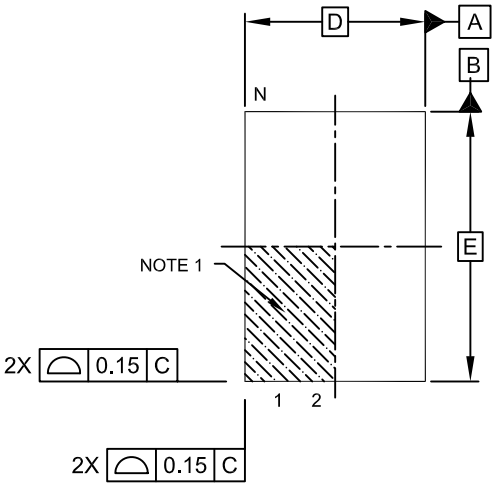
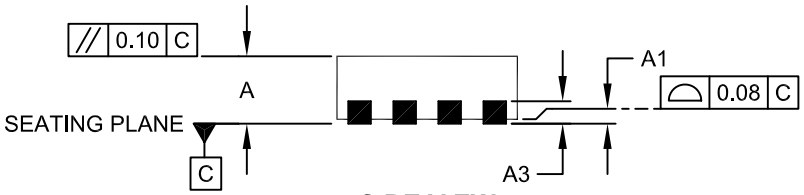
8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75mm Body [TDFN]

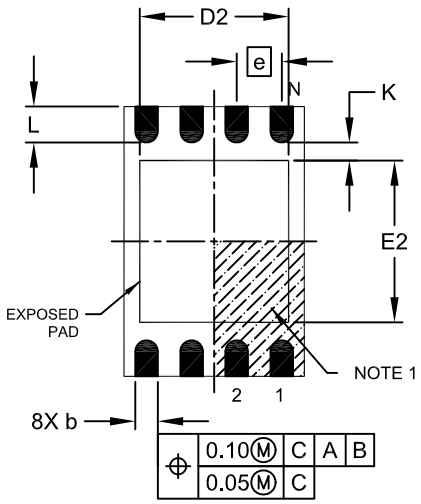
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Microchip Technology Drawing No. C04-129C Sheet 1 of 2

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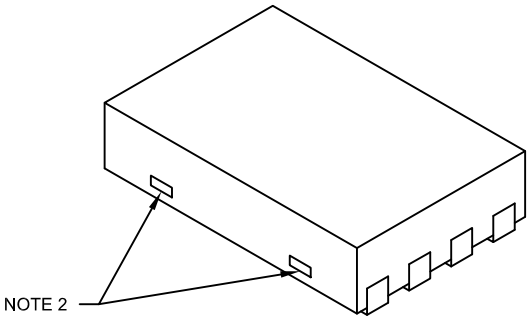
8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75mm Body [TDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.70	0.75	0.80
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		2.00 BSC	
Overall Width	E		3.00 BSC	
Exposed Pad Length	D2	1.20	-	1.60
Exposed Pad Width	E2	1.20	-	1.60
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.25	0.30	0.45
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-129C Sheet 2 of 2

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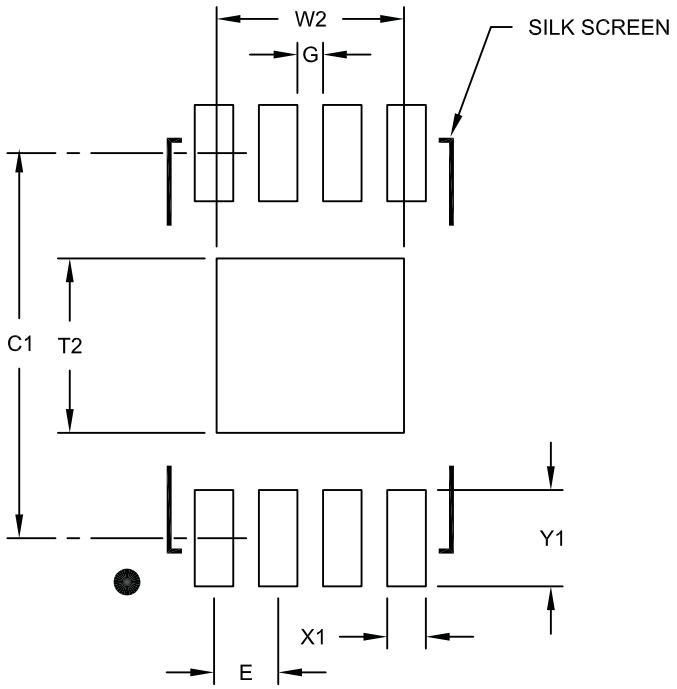
8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75 mm Body [TDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	W2			1.46
Optional Center Pad Length	T2			1.36
Contact Pad Spacing	C1		3.00	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2129A

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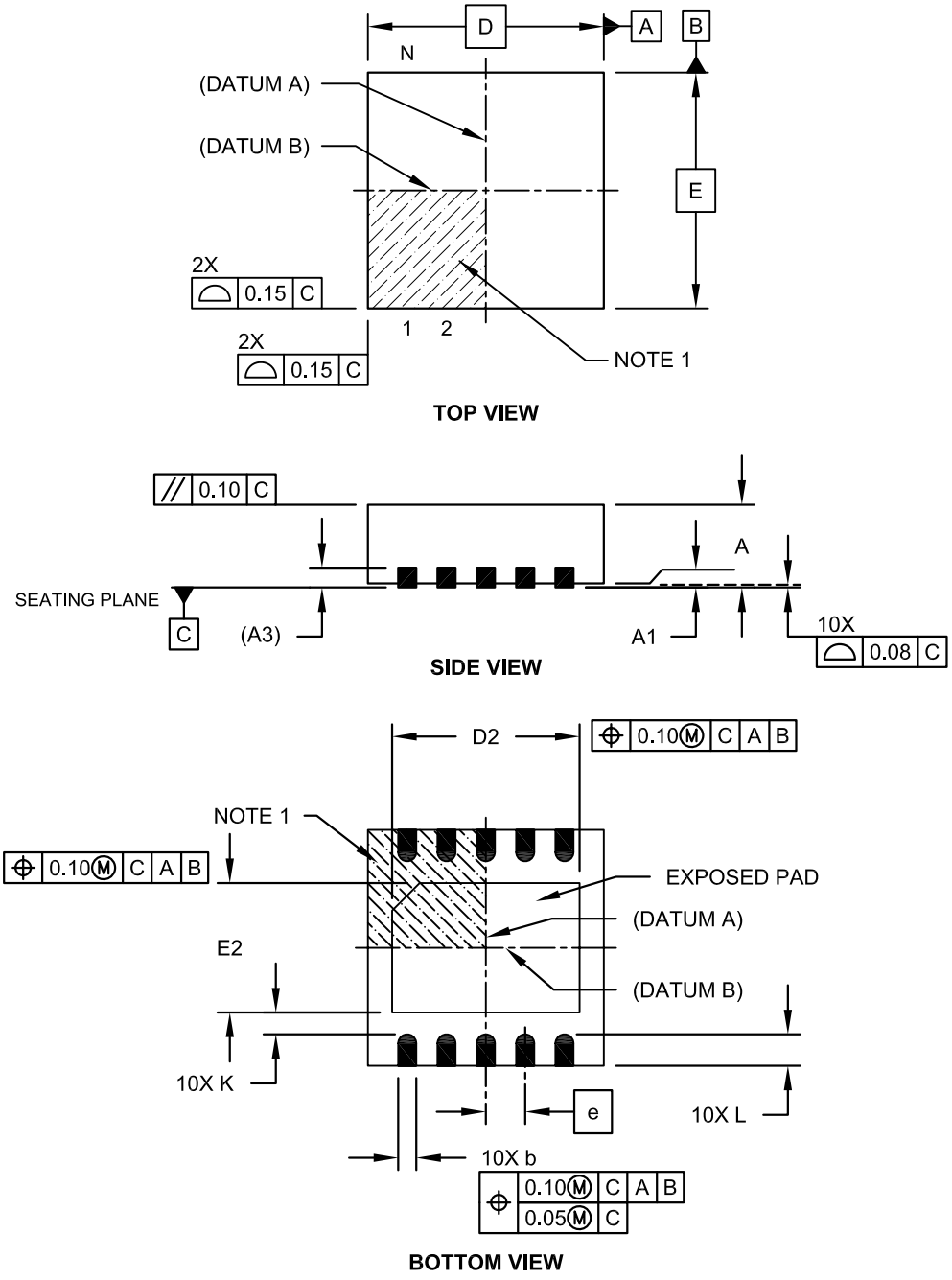
10-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-063C Sheet 1 of 2

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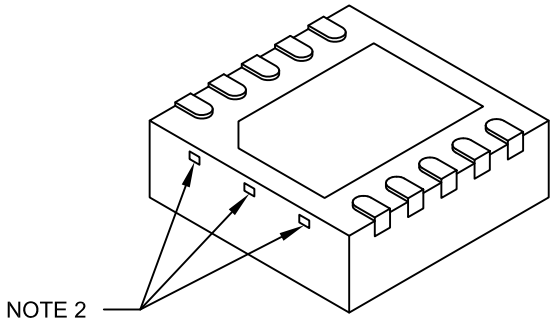
10-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		10	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		3.00 BSC	
Exposed Pad Length	D2	2.15	2.35	2.45
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.40	1.50	1.75
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-063C Sheet 2 of 2

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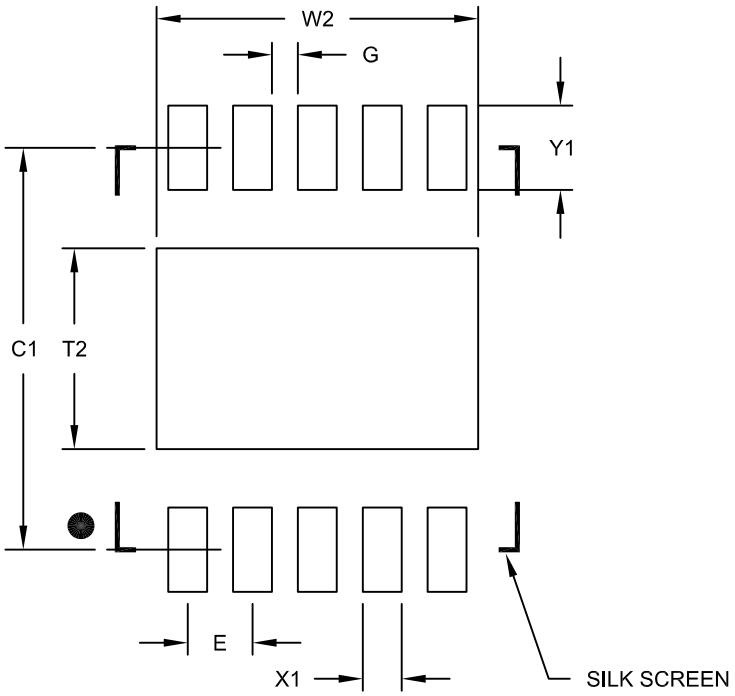
10-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	W2			2.48
Optional Center Pad Length	T2			1.55
Contact Pad Spacing	C1		3.10	
Contact Pad Width (X10)	X1			0.30
Contact Pad Length (X10)	Y1			0.65
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2063B

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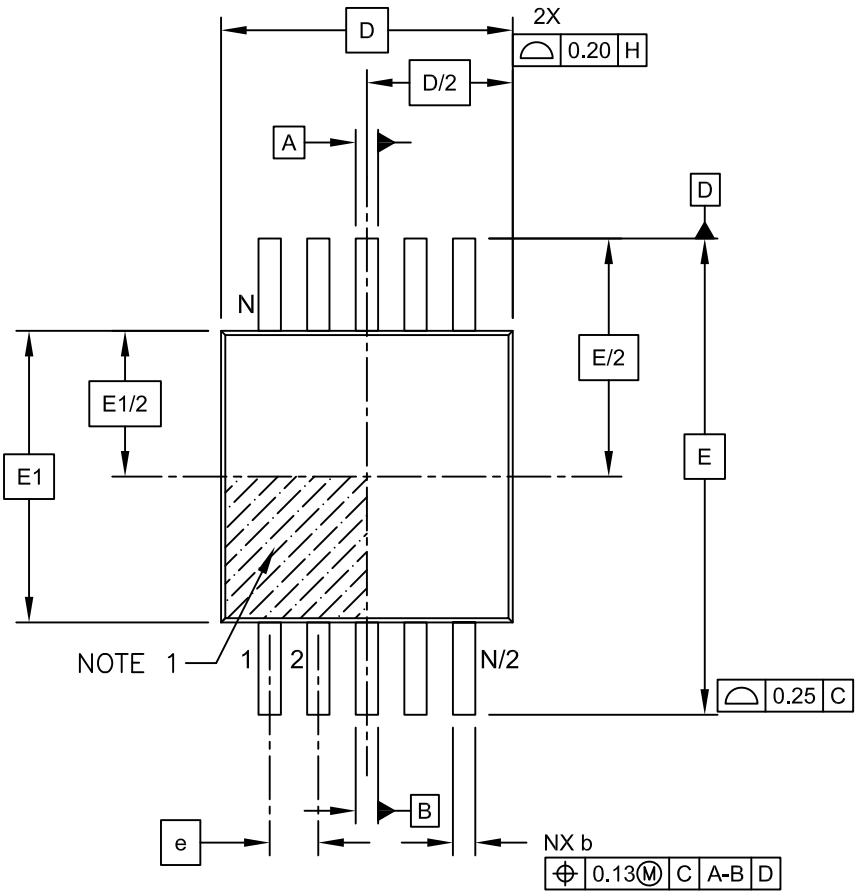
10-Lead Plastic Micro Small Outline Package (UN) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-021C Sheet 1 of 2

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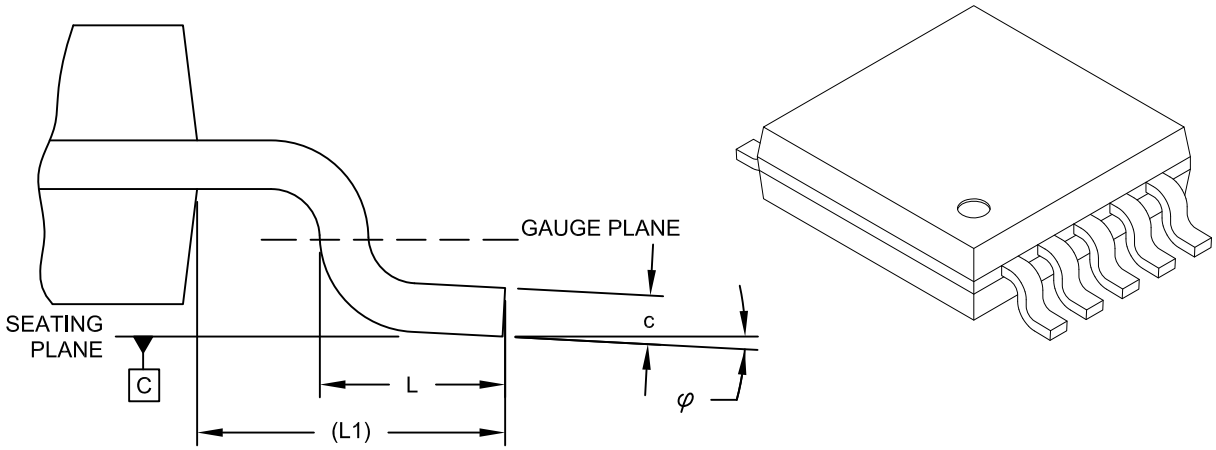
10-Lead Plastic Micro Small Outline Package (UN) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL C

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		10	
Pitch	e		0.50 BSC	
Overall Height	A	-	-	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	-	0.15
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Overall Length	D		3.00 BSC	
Foot Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.08	-	0.23
Lead Width	b	0.15	-	0.33

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-021C Sheet 2 of 2

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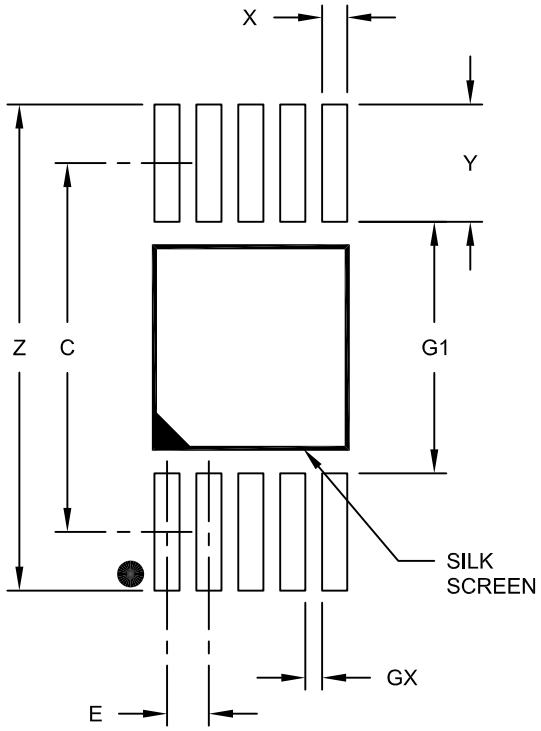
10-Lead Plastic Micro Small Outline Package (UN) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Contact Pad Spacing	C		4.40	
Overall Width	Z			5.80
Contact Pad Width (X10)	X1			0.30
Contact Pad Length (X10)	Y1			1.40
Distance Between Pads	G1	3.00		
Distance Between Pads	GX	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2021A

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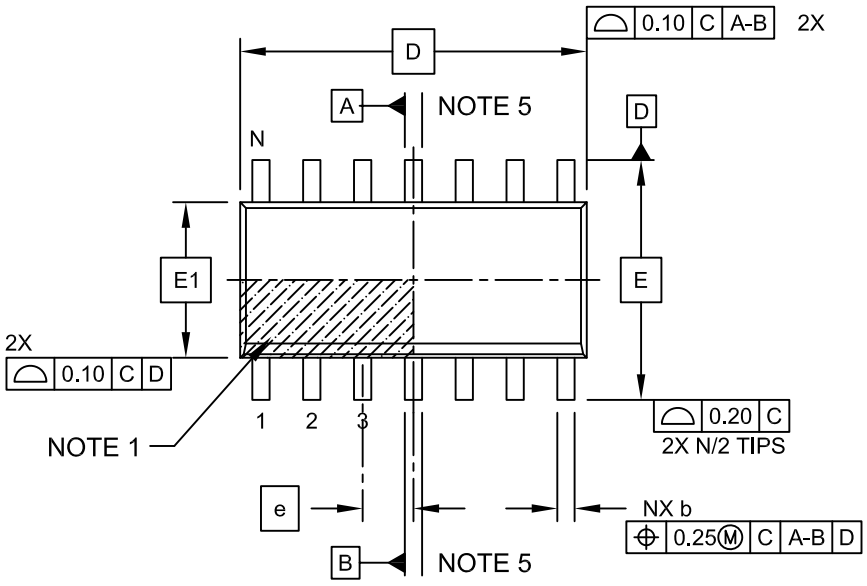
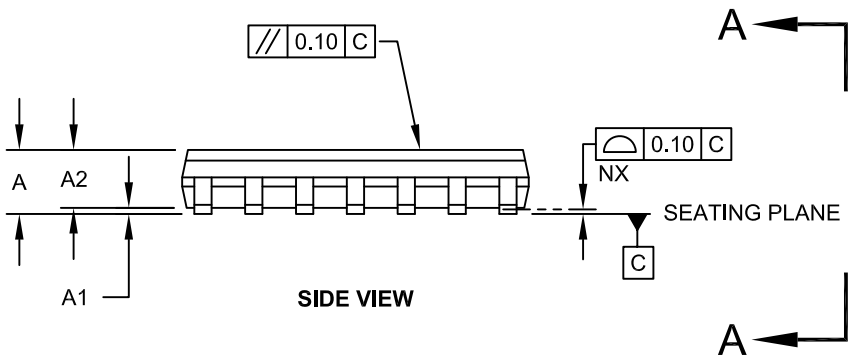
14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

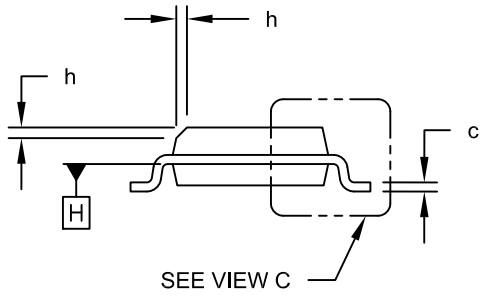
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW



VIEW A-A

Microchip Technology Drawing No. C04-065C Sheet 1 of 2

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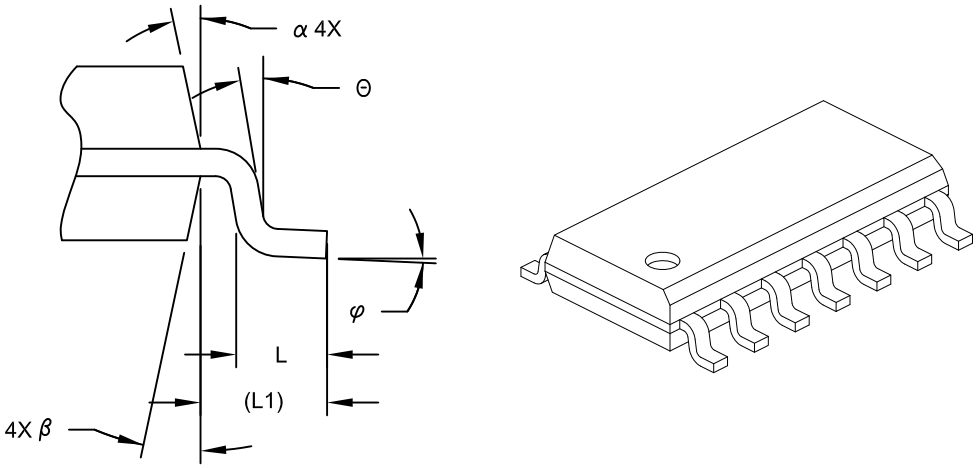
14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW C

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		8.65 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.10	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-065C Sheet 2 of 2

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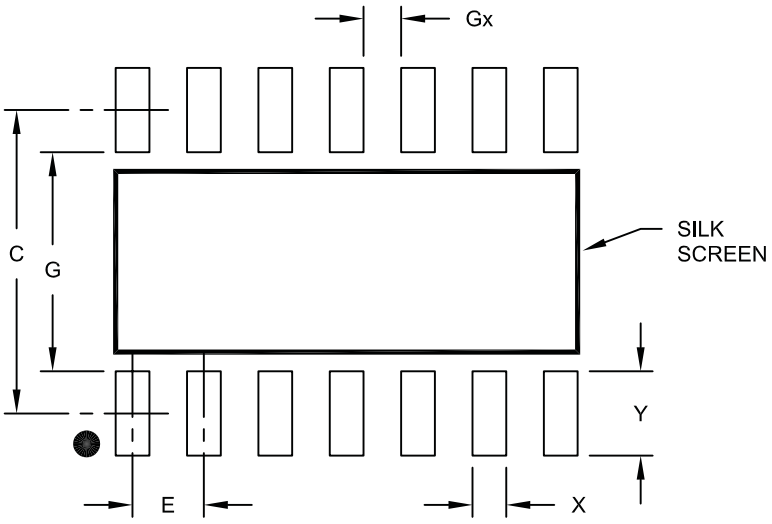
14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width	X			0.60
Contact Pad Length	Y			1.50
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	3.90		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2065A

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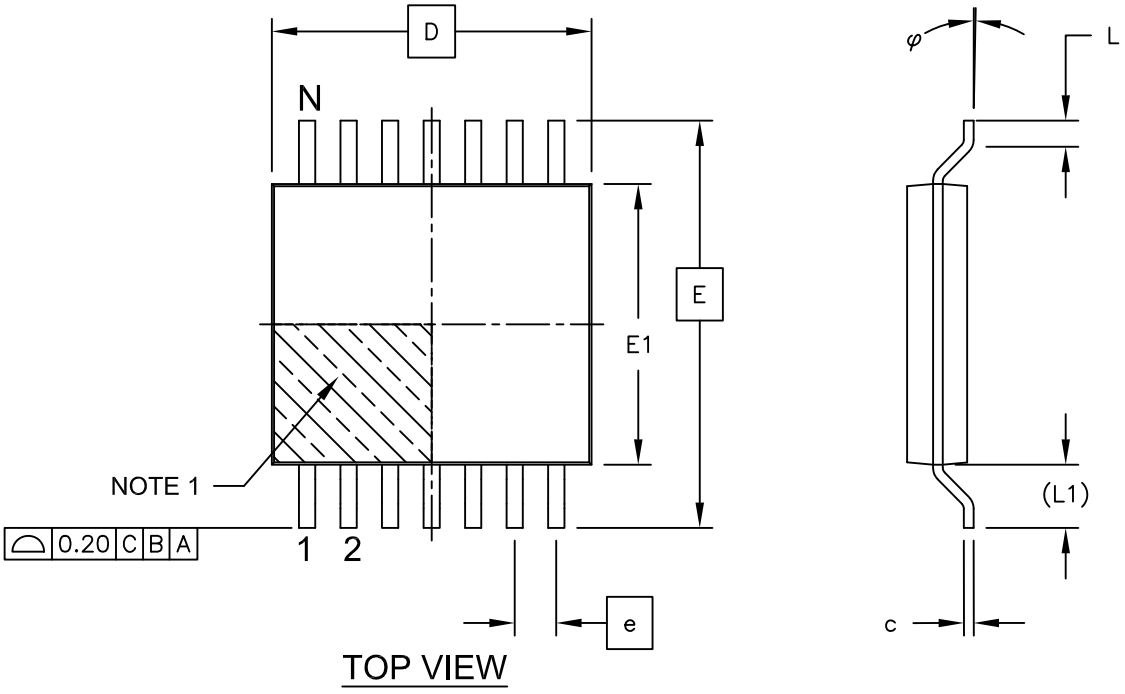
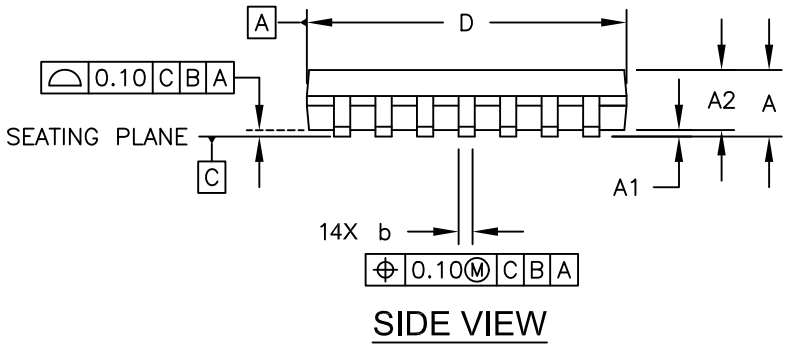
14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





Microchip Technology Drawing C04-087C Sheet 1 of 2

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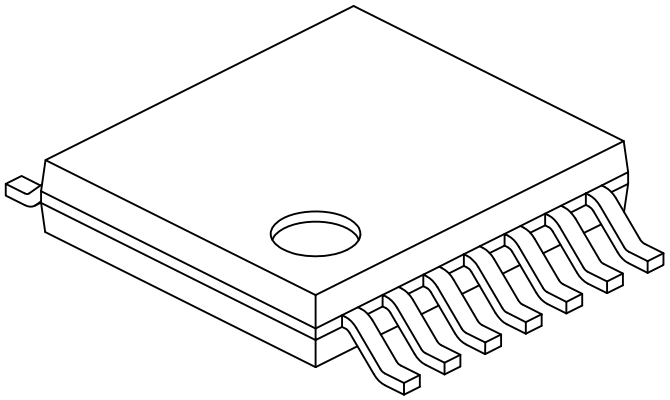
14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	-	0.15
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	4.90	5.00	5.10
Foot Length	L	0.45	0.60	0.75
Footprint	(L1)		1.00 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.09	-	0.20
Lead Width	b	0.19	-	0.30

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-087C Sheet 2 of 2

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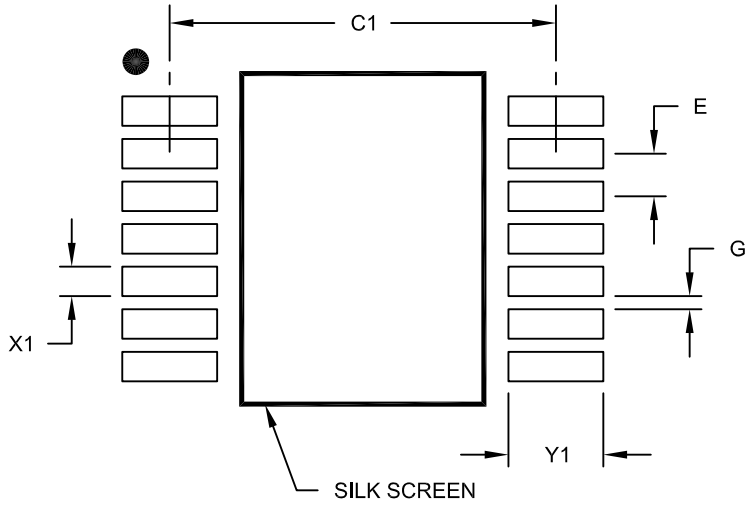
14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C1		5.90	
Contact Pad Width (X14)	X1			0.45
Contact Pad Length (X14)	Y1			1.45
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2087A

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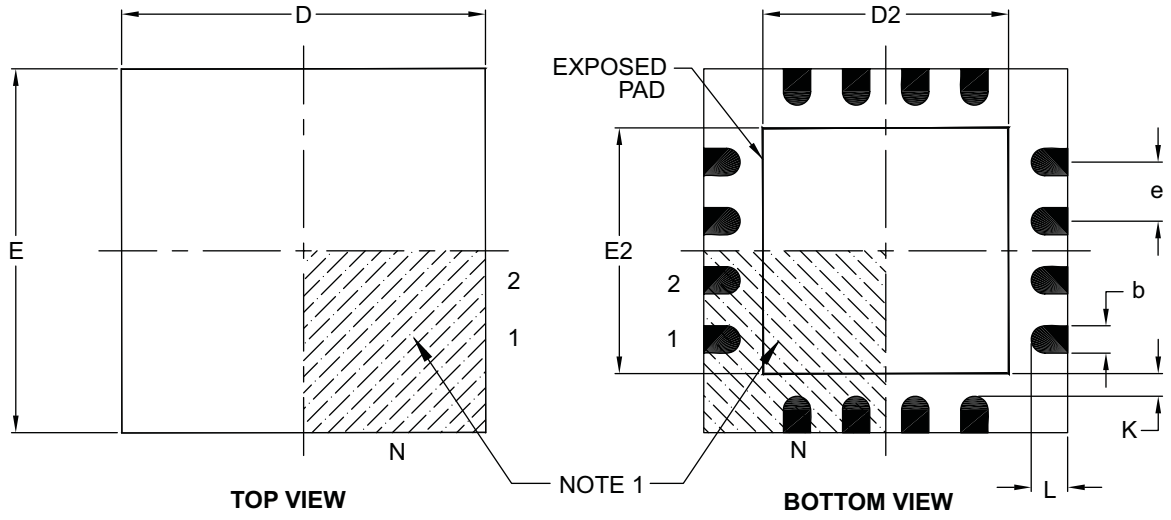
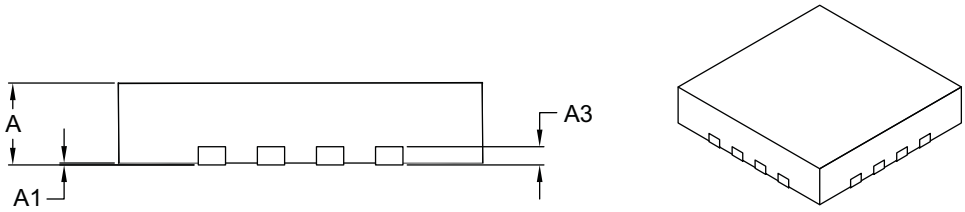
16-Lead Plastic Quad Flat, No Lead Package (ML) – 4x4x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		16	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.50	2.65	2.80
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.50	2.65	2.80
Contact Width	b	0.25	0.30	0.35
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-127B

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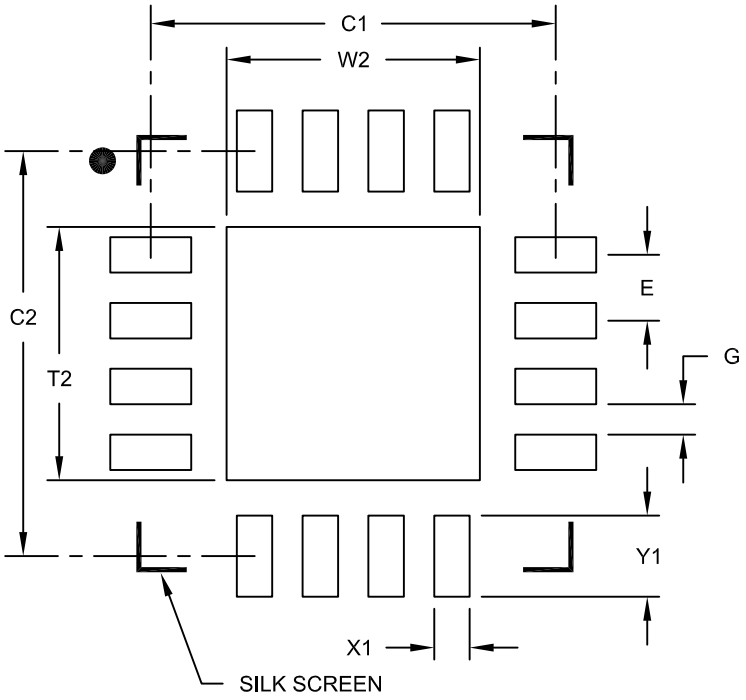
16-Lead Plastic Quad Flat, No Lead Package (ML) - 4x4x0.9mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	W2			2.50
Optional Center Pad Length	T2			2.50
Contact Pad Spacing	C1		4.00	
Contact Pad Spacing	C2		4.00	
Contact Pad Width (X16)	X1			0.35
Contact Pad Length (X16)	Y1			0.80
Distance Between Pads	G	0.30		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2127A

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APPENDIX A: REVISION HISTORY

Revision D (July 2014)

The following is a list of modifications:

1. Updated the title of the document.
2. Added the High Gain-Bandwidth Op Amp Portfolio table and updated all sections on page 1.

Revision C (June 2011)

The following is a list of modifications:

3. Added the 2x3 TDFN (8L) package option for MCP651, SOT-23 (5L) package for MCP651S and SOT-23 (6L) package option for MCP653 and the related information throughout the document.

Revision B (March 2011)

The following is a list of modifications:

1. Added the MCP654 and MCP659 amplifiers to the product family and the related information throughout the document.
2. Added the corresponding SOIC (14L), TSSOP (14L) and QFN (16L) package options and related information.

Revision A (April 2009)

- Original Release of this Document.

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	-X	/XX
Device	Temperature Range	Package

Device:	MCP651:	Single Op Amp
	MCP651T:	Single Op Amp (Tape and Reel) (SOIC)
	MCP651S:	Single Op Amp (SOT)
	MCP652:	Dual Op Amp
	MCP652T:	Dual Op Amp (Tape and Reel) (DFN and SOIC)
	MCP653T:	Single Op Amp (Tape and Reel) (SOT)
	MCP654:	Quad Op Amp
	MCP654T:	Quad Op Amp (Tape and Reel) (TSSOP and SOIC)
	MCP655:	Dual Op Amp
	MCP655T:	Dual Op Amp (Tape and Reel) (DFN and MSOP)
	MCP659:	Quad Op Amp
	MCP659T:	Quad Op Amp (Tape and Reel) (QFN)
Temperature Range:	E =	-40°C to +125°C
Package:	OT =	Plastic Small Outline, (2x3 SOT), 5-lead
	CHY =	Plastic Small Outline, (2x3 SOT), 6-lead
	SN =	Plastic Small Outline, (3.90 mm), 8-lead
	MNY =	Plastic Dual Flat, (2x3 TDFN), 8-lead
	MF =	Plastic Dual Flat, No Lead (3x3 DFN), 8-lead, 10-lead
	UN =	Plastic Micro Small Outline, (MSOP), 10-lead
	ST =	Plastic Thin Shrink Small Outline, (4.4 mm), 14-lead
	SL =	Plastic Small Outline, Narrow, (3.90 mm), 14-lead
	ML =	Plastic Quad Flat, No Lead Package, (4x4x0.9 mm), 16-lead

* Y = Nickel palladium gold manufacturing designator. Only available on the TDFN package.

Examples:

a) MCP651ST-E/OT: Tape and Reel, Extended Temperature, 5LD SOT package.

b) MCP651T-E/SN: Tape and Reel, Extended Temperature, 8LD SOIC package.

c) MCP651T-E/MNY: Tape and Reel, Extended Temperature, 8LD TDFN package.

d) MCP652T-E/MF: Tape and Reel, Extended Temperature, 8LD DFN package.

e) MCP652T-E/SN: Tape and Reel, Extended Temperature, 8LD SOIC package.

f) MCP653T-E/CHY: Tape and Reel, Extended Temperature, 6LD SOT package.

g) MCP654T-E/SL: Tape and Reel, Extended Temperature, 14LD SOIC package.

h) MCP654T-E/ST: Tape and Reel, Extended Temperature, 14LD TSSOP package.

i) MCP655T-E/MF: Tape and Reel, Extended Temperature, 10LD DFN package.

j) MCP655T-E/UN: Tape and Reel, Extended Temperature, 10LD MSOP package.

k) MCP659T-E/ML: Tape and Reel, Extended Temperature, 16LD QFN package.

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